Strongbow_KL
Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

<Core Design>

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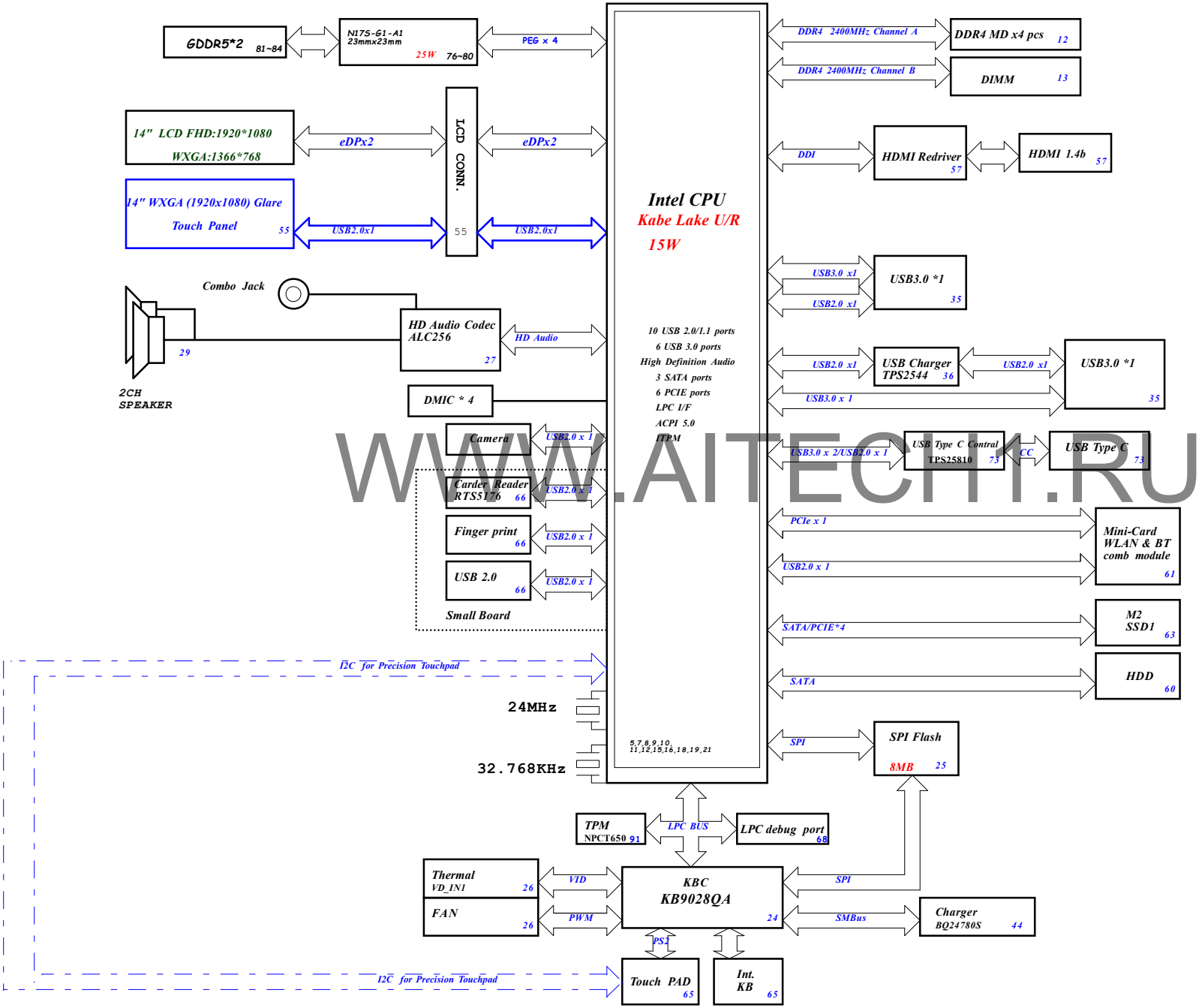
Project Code:4PD0E7010001
PCB No :17863
Revision : 1

Strongbow_KBL Block Diagram



GPU DC/DC RT8813DGQW-GP 85	
INPUTS	OUTPUTS
5V_S0	1V_VGACORE_S0

GPU DC/DC RT8816AGQW-GP 86	
INPUTS	OUTPUTS
5V_S5	1D35V_VGA_S0

GPU DC/DC SY8003ADFC-GP 86	
INPUTS	OUTPUTS
3D3V_S5	1D8V_AON_S0

GPU DC/DC APE8939GN3-GP 86	
INPUTS	OUTPUTS
1D8V_AON_S0	1D8V_VGA_S0

GPU DC/DC APE8939GN3-GP 86	
INPUTS	OUTPUTS
1D0V_S5	1V_1D05V_VGA_S0

CHARGER BQ24780S 44	
INPUTS	OUTPUTS
AD+ BT+	19V_DCBATOUT

SYSTEM DC/DC RT6258CGQUF-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 5V_S5

SYSTEM DC/DC RT6256BGQUF-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_S5

CPU DC/DC RT3602 46-47	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC AOZ5049 48	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VCCGT

CPU DC/DC RT9610B 50	
INPUTS	OUTPUTS
5V_S5	1V_VCCSA

CPU DC/DC G5388K11U-GP 51	
INPUTS	OUTPUTS
5V_S5	PWR_VDDQ

CPU DC/DC APL5930KAI 51	
INPUTS	OUTPUTS
5V_S5	2D5V_S3

SYSTEM DC/DC G5388K11U-GP 52	
INPUTS	OUTPUTS
5V_S5	1D0V_S5

SYSTEM DC/DC G9661-25ADJ 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM Load switch TPS22976 40	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
5V_S5	5V_S0
1D0V_S5	1V_VCCST
1D8V_S5	1D8V_S0

SYSTEM Load switch APE8939 40	
INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO

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Main Func = CPU

eDP

[55] eDP_TX_CPU_N0
[55] eDP_TX_CPU_P0
[55] eDP_TX_CPU_N1
[55] eDP_TX_CPU_P1

[55] eDP_AUX_CPU_P
[55] eDP_AUX_CPU_N

[55] eDP_HPD_CPU
[24] eDP_BLEN_CPU
[55] eDP_BLCTRL_CPU
[55] eDP_VDDEN_CPU

HDMI

[57] HDMI_DDI_TX_N2
[57] HDMI_DDI_TX_P2
[57] HDMI_DDI_TX_N1
[57] HDMI_DDI_TX_P1
[57] HDMI_DDI_TX_N0
[57] HDMI_DDI_TX_P0
[57] HDMI_DDI_TX_N3
[57] HDMI_DDI_TX_P3

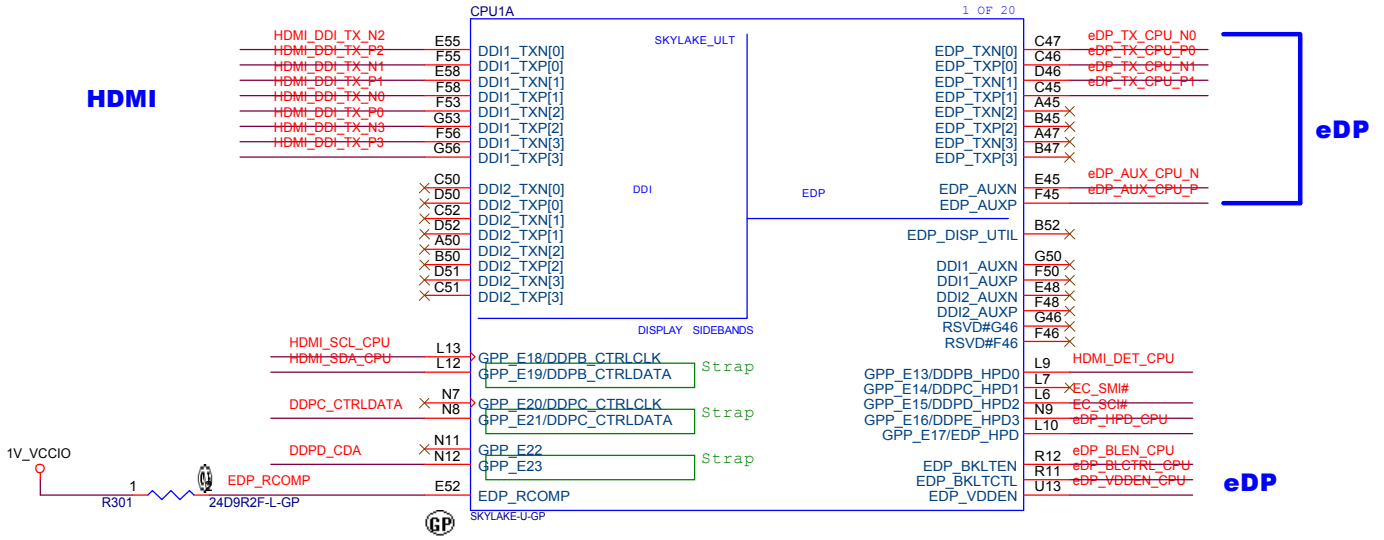
[15,57] HDMI_SCL_CPU
[15,57] HDMI_SDA_CPU

[57] HDMI_DET_CPU

STRAP

[15] DDPC_CTRLDATA
[15] DDPD_CDA

[24] EC_SCI#



(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ± 1%	Max = 100 mils

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ± 1% Ω resistor

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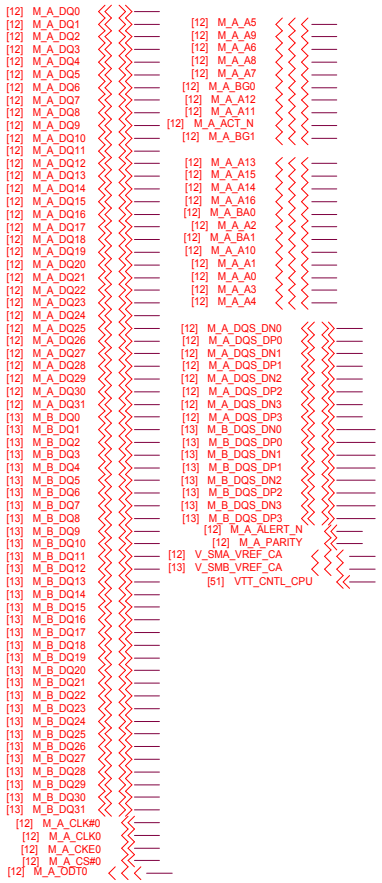
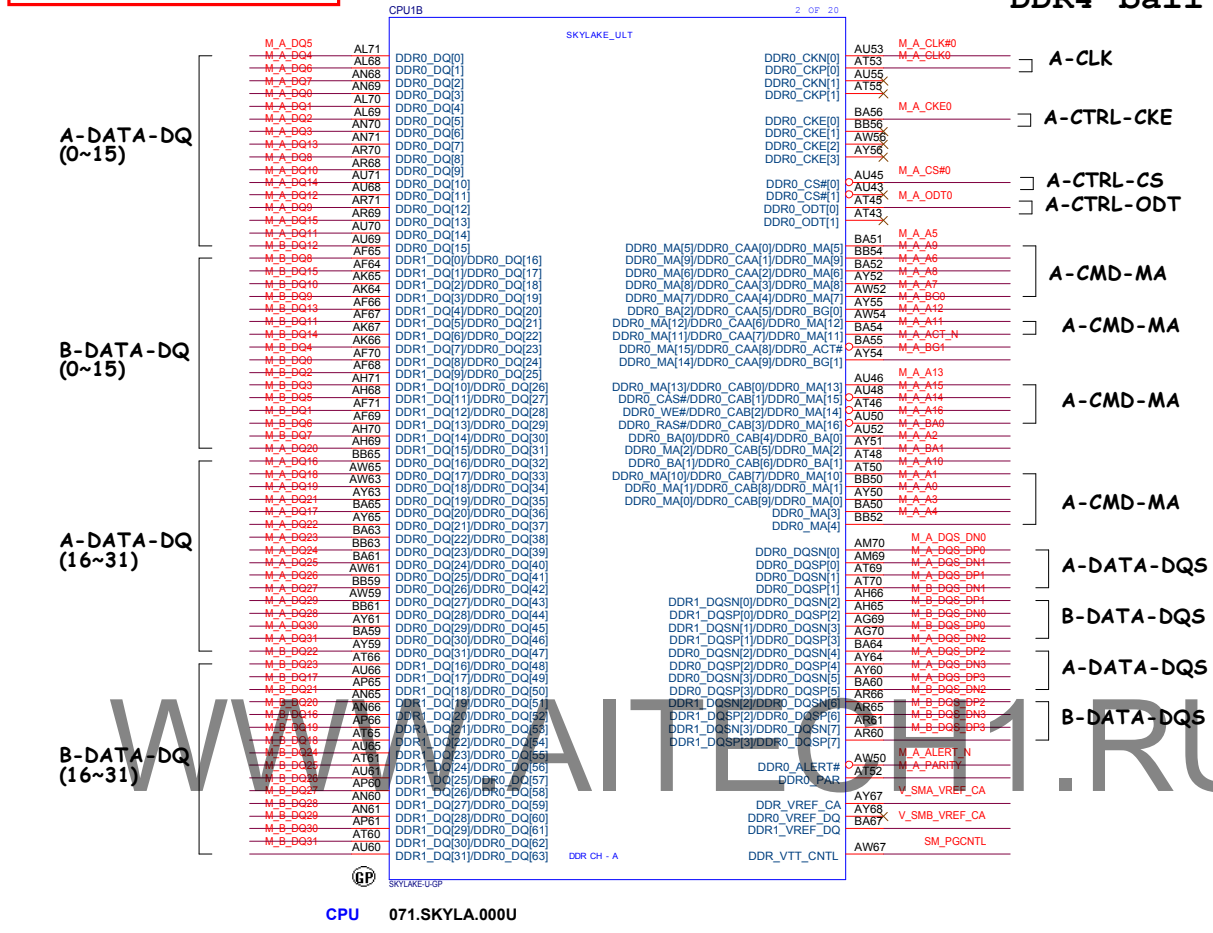
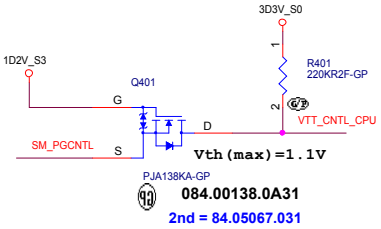
Main Func = CPU

DDR4 ball type:Interleaved Type







CPU 071.SKYLA.000U

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Title: CPU_(DDR)

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Main Func = CPU

DDR4 ball type:Interleaved Type

A-DATA-DQ (32~47)

B-DATA-DQ (32~47)

A-DATA-DQ (48~63)

B-DATA-DQ (48~63)

B-CLK

B-CTRL-CKE

B-CTRL-CS

B-CTRL-ODT

B-CMD-MA

B-CMD-MA

B-CMD-MA

B-CMD-MA

A-DATA-DQS

B-DATA-DQS

A-DATA-DQS

B-DATA-DQS

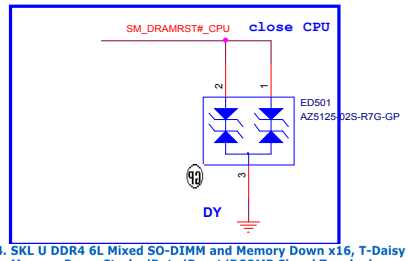
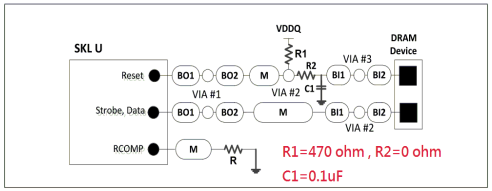


Figure 5-14. SKL U DDR4 6L Mixed SO-DIMM and Memory Down x16, T-Daisy Topology Memory Down Strobe/Data/Reset/RCOMP Signal Topologies



071.SKYLA.000U

CPU

#543016

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

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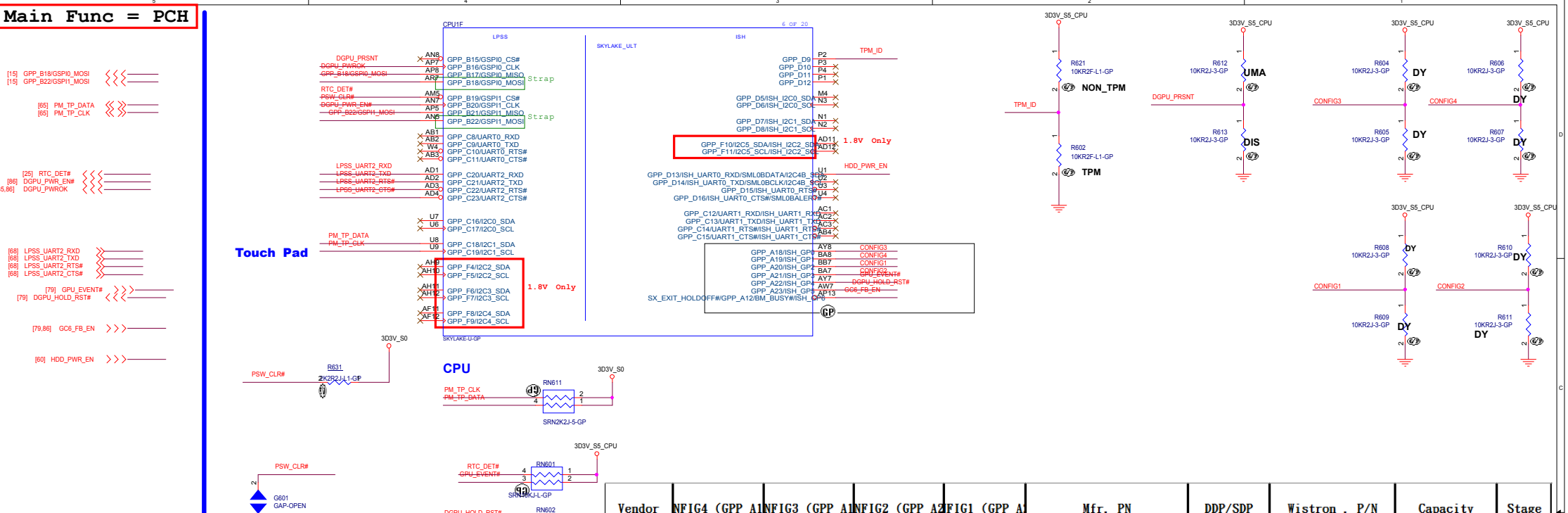
Main Func = PCH



Vendor	NFIG4 (GPP_A1	NFIG3 (GPP_A1	NFIG2 (GPP_A2	FIG1 (GPP_A1	Mfr. PN	DDP/SDP	Wistron . P/N	Capacity	Stage
HYNIX	0	0	0	0	H5AN8G6NAFR-UHC	SDP	KN.8GB0G.049	8Gb	
Micron	0	0	0	1	MT40A512M16LY-075	SDP	KN.8GB04.027	8Gb	LAB
Micron	0	0	1	0	MT40A1G16KNR-075	DDP	KN.01604.003	16Gb	LAB
HYNIX	0	0	1	1	H5ANAG6NAMR-UHC	DDP	KN.0160G.010	16Gb	

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

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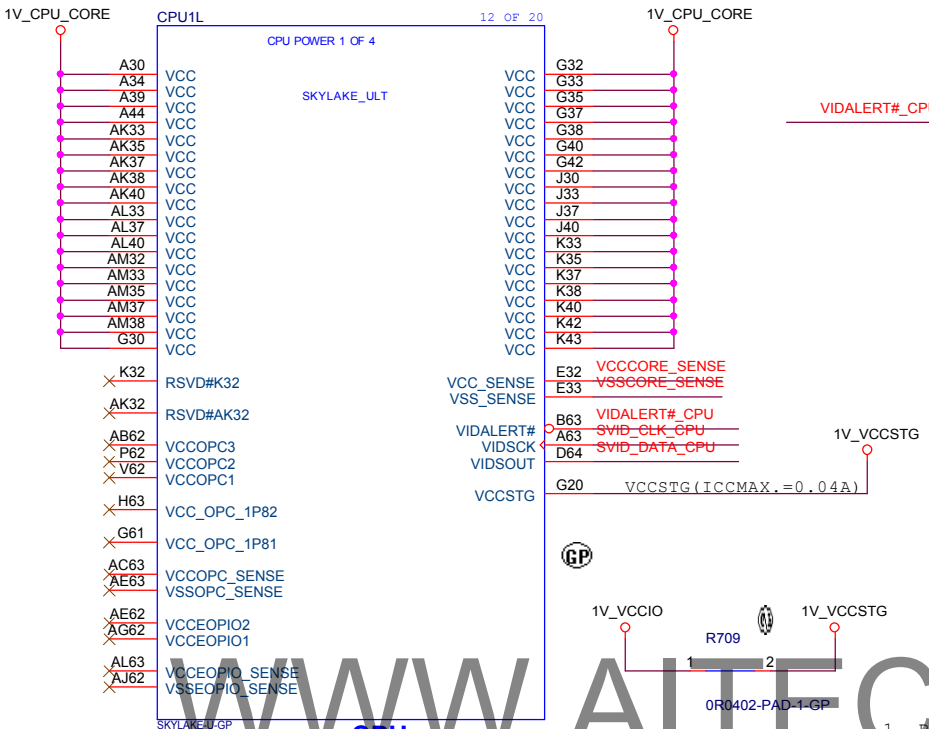
Main Func = CPU

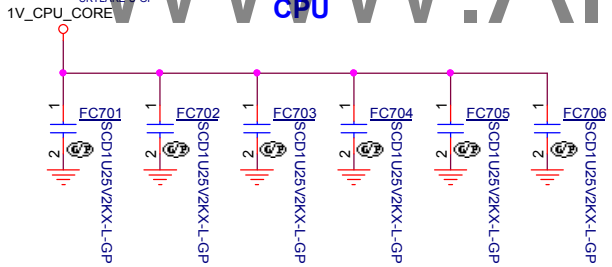
SVID

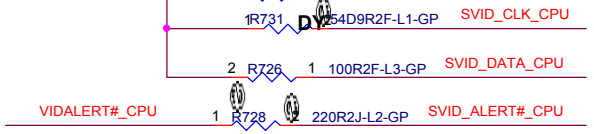
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU

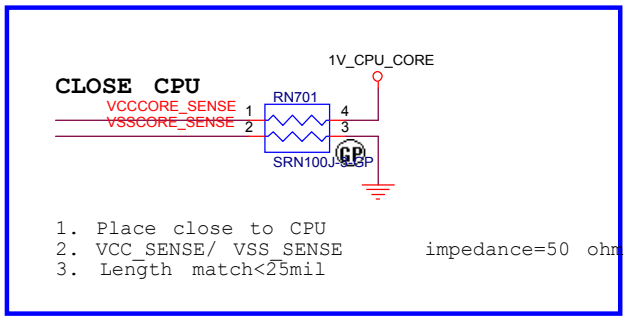
[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE
[7,46] SVID_ALERT#_CPU
[7,46] SVID_CLK_CPU
[7,46] SVID_DATA_CPU
[7,46] VCCCORE_SENSE
[7,46] VSSCORE_SENSE



CPU







Layout Note:
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Length match<25mil

Figure 10-7. Routing Illustration for SVID Topology

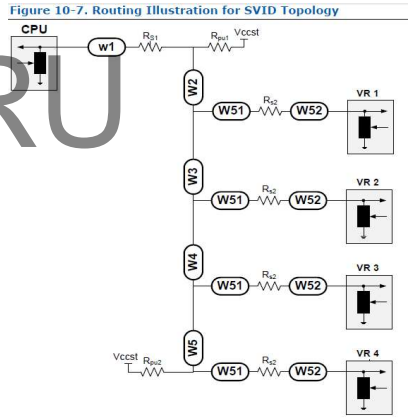


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT#							56	Empty	220	0	

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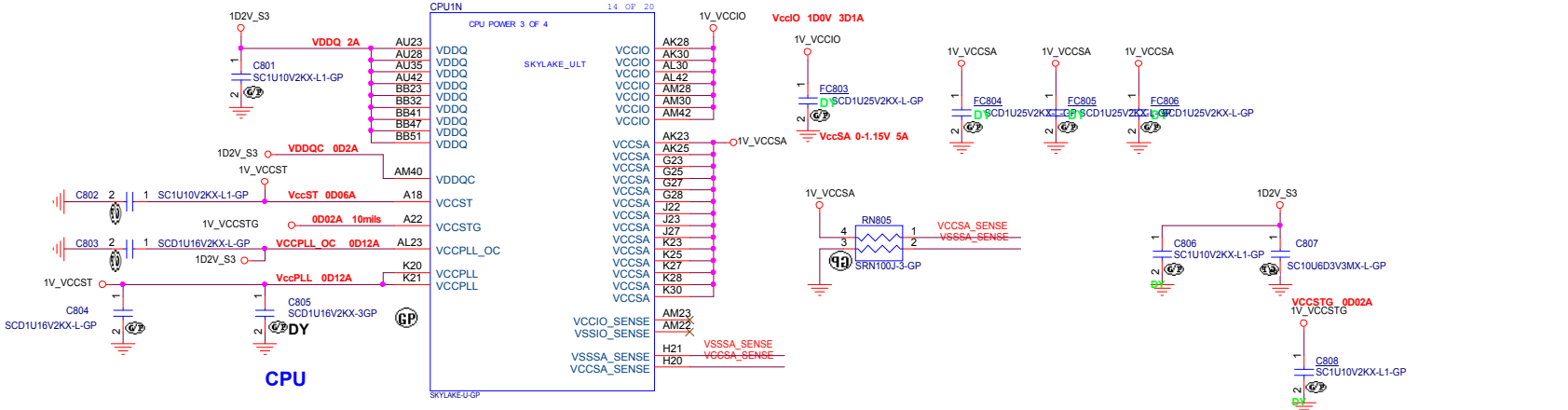
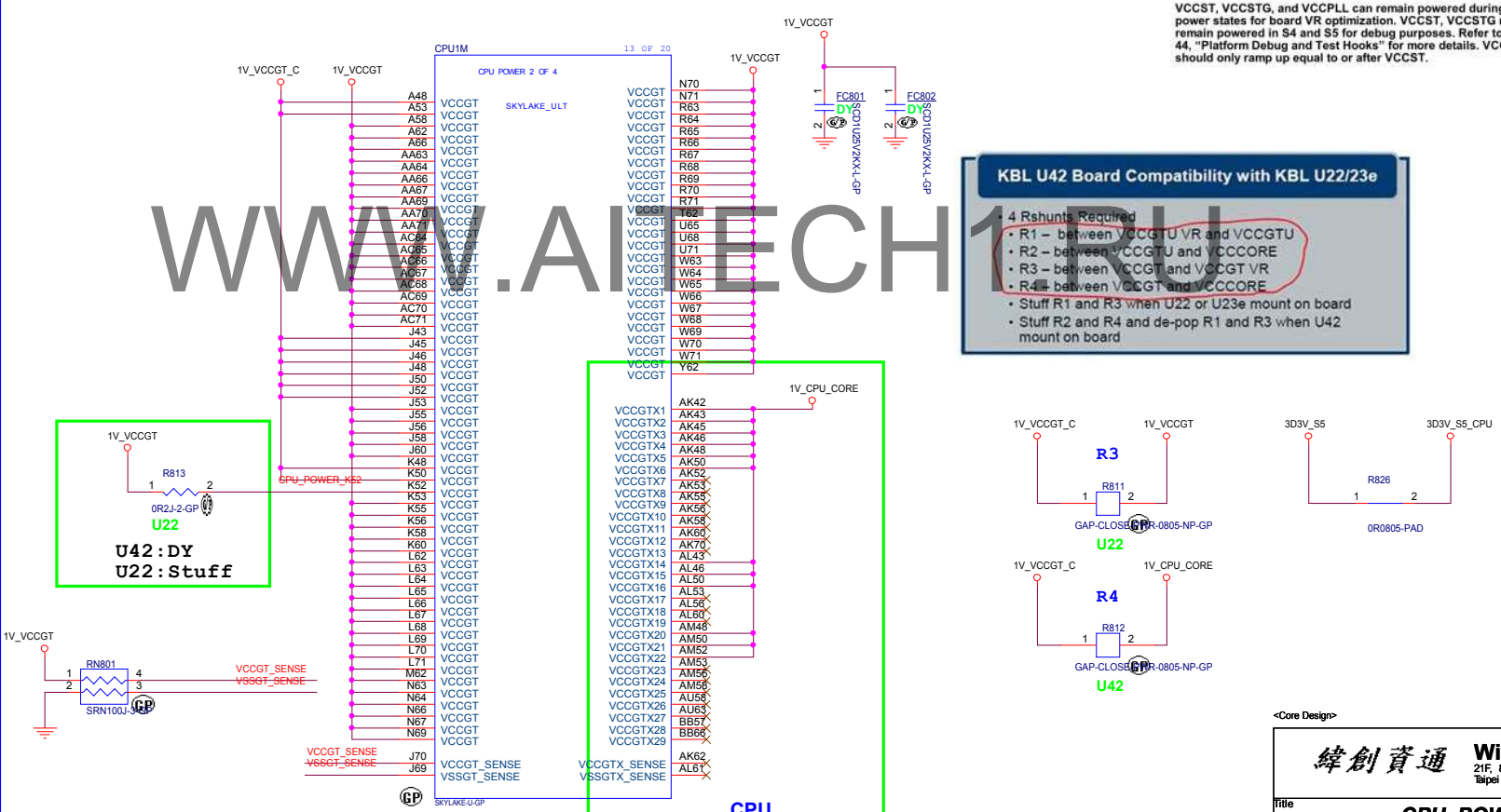
Main Func = CPU

[46] VSSSA_SENSE
[46] VCCSA_SENSE
[46] VCCGT_SENSE
[46] VSSGT_SENSE



VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 44, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.



U42 and U22 power co-lay

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Blanking

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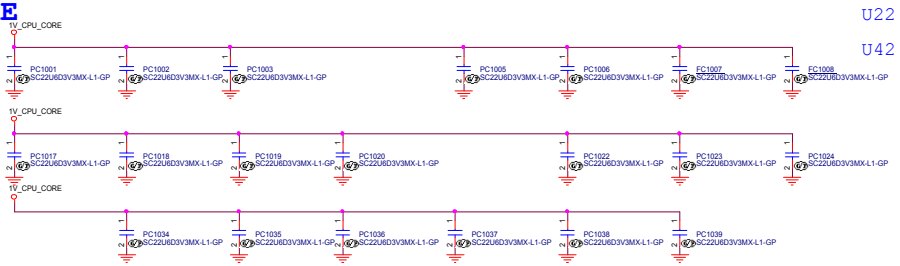
Main Func = CPU

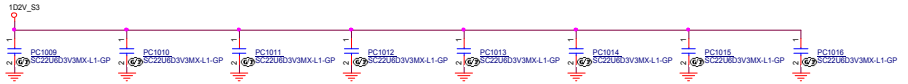
VCORE

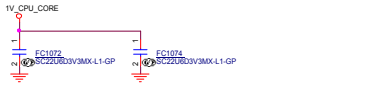
1V_CPU_CORE

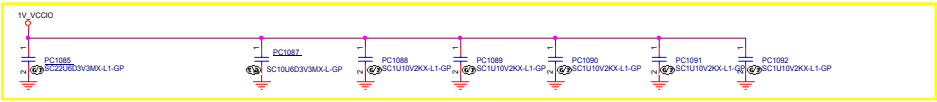
U22 0603 22uF *25 , 0603 10uF*1

U42 0603 22uF *12



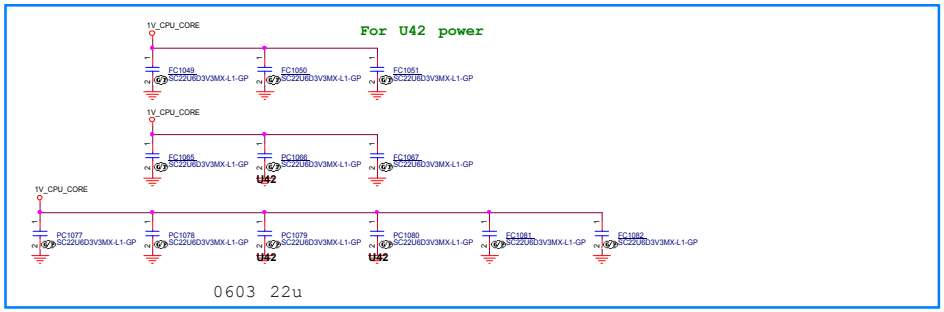






1V_VCCIO

22uF* 1 10uF * 1 1uF *4



Power Layout

48.1.3 Kaby Lake U Compatible Design Recommendation

48.1.3.1 KBL-R U 4+2 / KBL U 2+2 Design Recommendation

Table 48-3. Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)		Placed at backside side near to VR output
V_{CCGT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V_{CCIO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V_{CCSA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
V_{CCPLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

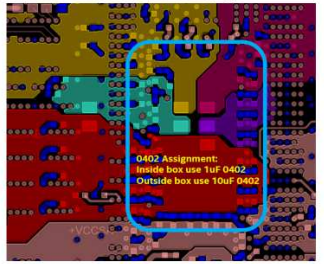
Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 1 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/V_{CCGT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
V_{CCGT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	

Table 48-4. Decoupling Requirements for KBL-R U 4+2 / KBL U 2+2 Processor (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
V_{CCSA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
V_{CCIO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
V_{CCPLL}		1 x 1 uF 0402	Place as close to the package as possible.
V_{CCPLL_OC}		1 x 1 uF 0201	Do not route V_{CCPLL}, V_{CCPLL_OC}, V_{CCGT} closest adjacent layer over any power net other than ground.
V_{CCST}		1 x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ' 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Due to the difference between the package designs, KBL U 2+2 design requires more on-board decoupling in order to maintain the same loadline.
4. Diagram of placement for 0402 backside caps for CPU decoupling.



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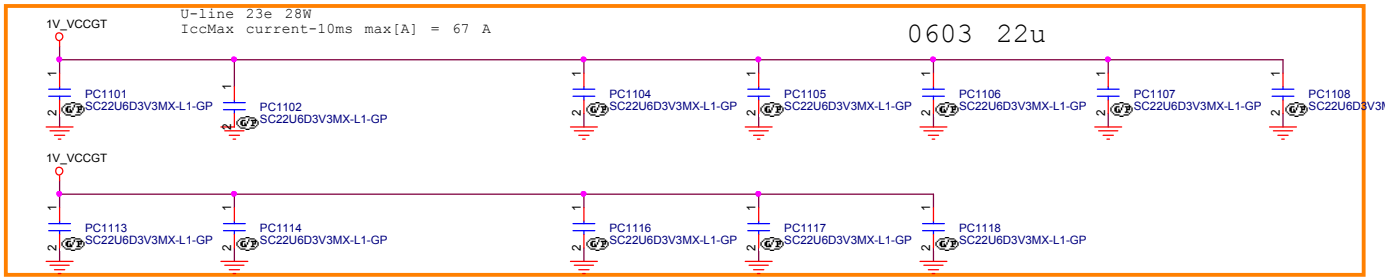
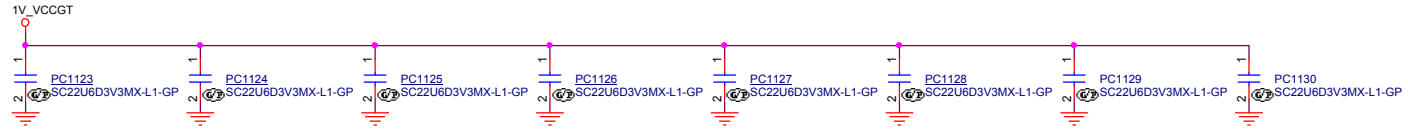
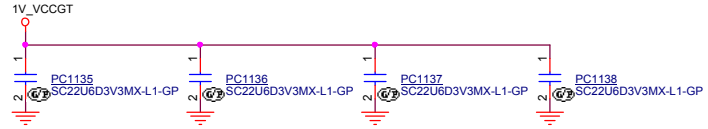
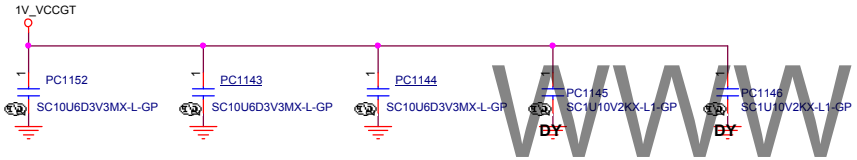
Main Func = CPU

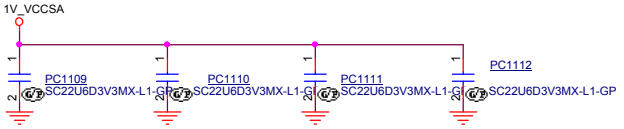
SLICED GT

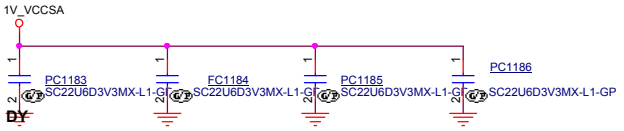


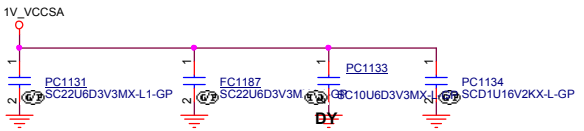


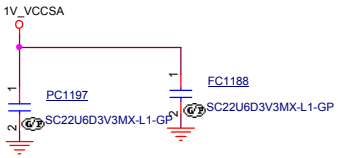




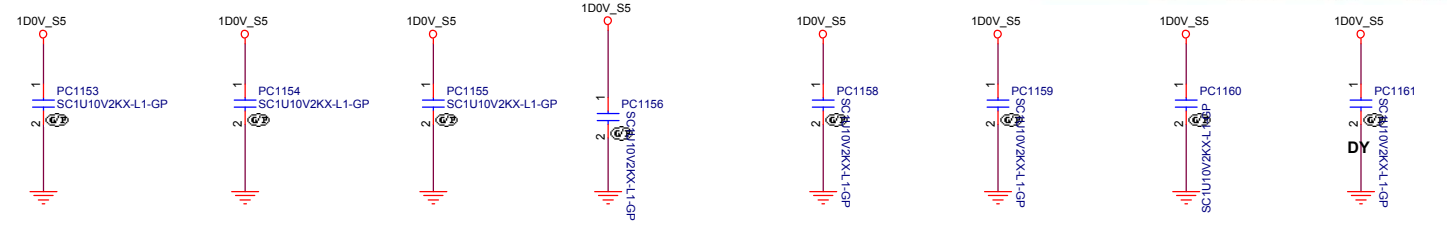


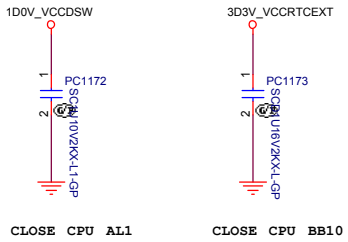


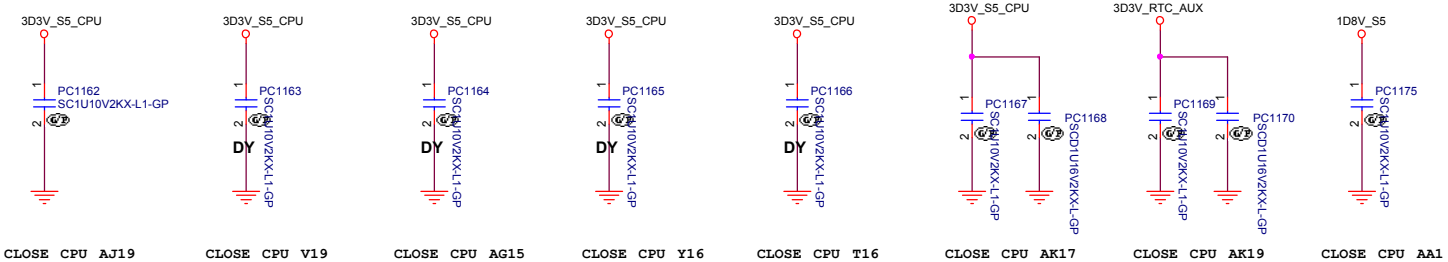




U22 15W	IA	750MHz	33A (28A)	23A (21A)	2.1mΩ (2.35mΩ)	30A (TBD)	200mv/30us	1X0.15uH	2X330uF/9mW	30X22uF
								Or	1x330uF/9mW	36x22uF
	GT	750KHz	40A(31A)	18A (18A)	3.1mΩ	38A (TBD)	70mv/10us	1X0.15uH	2X330uF/9mW	24X22uF
								Or	1x330uF/9mW	36x22uF
	SA	750KHz	6A (5A)	6A (4A)	10.3mΩ	4A (TBD)	200mv/30us	1X0.42uH	None	5X22uF





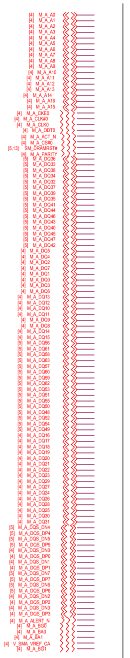


<Core Design>

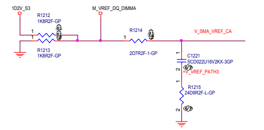
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU_(Power CAP2)
Size A3 / Document Number	Strongbow_KL / Rev 1
Date: Monday, January 15, 2018	Sheet 11 of 106

SSID = DDR4 CHA

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63



please notice that signal BG1 (pin:M9) and UZQ (pin:E9) are required



SDP & DDP SETTING

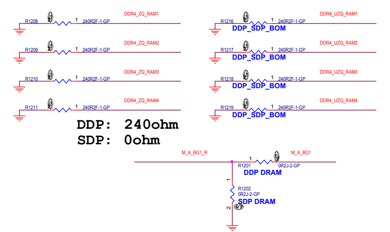
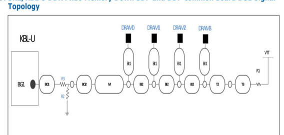


Figure 3-29. SKL/KBL U DDR4 x16 Memory Down SDP and DDP common board BG1 Signal Topology



Note: When DDP: R3 = 0 ohms/0201/1%, R2 = Unstuffed

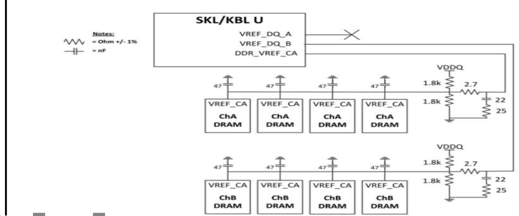
Note: When SDP: R3 = Unstuffed , R2 = 0 ohms

Note: BO1+ BO2 + M should be 25mils shorter than other CMD signals.

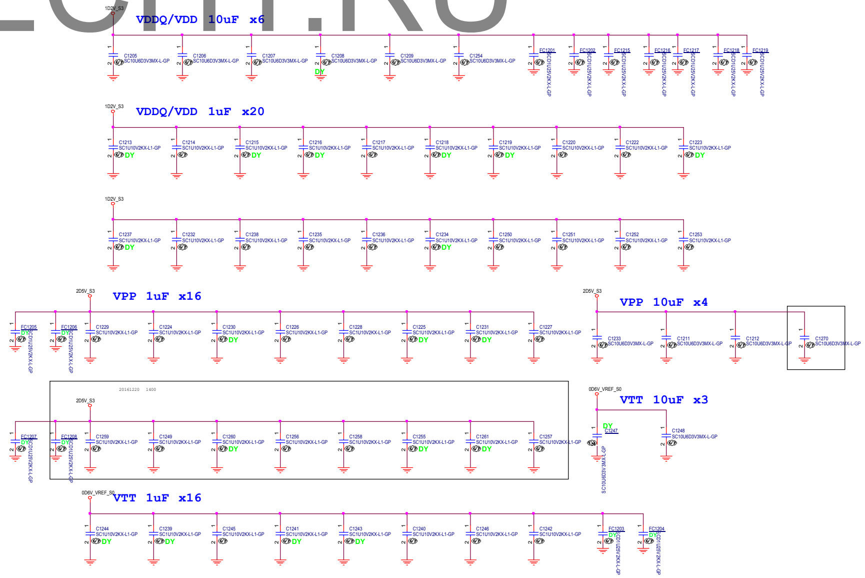
DDP x16 and SDP x16 Compatible Layout

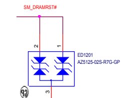
- Alternate two layout, risk of VSS offset increases a little

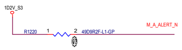
Figure 4-3. SKL/KBL U DDR4 Memory Down V_{REF-DQ} and V_{REF-CA} Overview

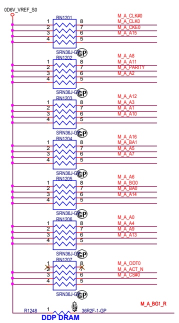


DDR4 On Board RAM Power Decouple Cap









4.14.3 KBL-R DDR4 Memory Down Decoupling

This recommendation assumes a 2Ch memory down implementation.

Table 4-27. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1µF (0402) (All stuffed)	
		Distributed around the DRAM devices	10x 10µF (0603) (All stuffed)	
	VPP	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	5x 10µF (0603)	
	VTT	2 as near each x16 DRAM device as possible	16x 1µF (0402)	
		Distributed around the DRAM devices	4x 10µF (0603)	

For ODIMM1,ODIMM2,ODIMM3,ODIMM4

Wistron Corporation

LPDDR3L_CHA

Strongbow_KL

Rev 1

SSID = DDR4 CHB

All VREF traces should have width=20mil; spacing=20 mil

Layout Note:

Reverse Type

Note:
SO-DIMMB SPD Address is 0xA4

Place these Caps near DIMM2.

DIMM1A 1 OF 4 — DDR4-260P-6-GP

DIMM1C 3 OF 4 — DDR4-260P-6-GP

DIMM1B 2 OF 4 — DDR4-260P-6-GP

DIMM1D 4 OF 4 — DDR4-260P-6-GP

2nd = 062.10011.0C61

3rd = 062.10011.0D21

Thermal EVENT

1D2V_S3 — R1303 240R2F-1-GP — TS#_DIMM1_1 — DY

SPD Address of XMM1

SPD SA1	1
SPD SA0	0

need close to PIN 255

3D3V_S0 — C1306 — C1305 — DY

M_VREF_CA_DIMMB — RN1301 SRN1KJ-7-GP — R1305 2R2F-GP — V_SMB_VREF_CA

C1328 SCD022U16V2KX-3GP — +V_VREF_PATH2

R1306 24D9R2F-L-GP

C1302 SCD1U16V2KX-L-GP

Layout Note: Place these caps close to DM2 PIN1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LPDDR3L_CHB

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 13 of 106

<Core Design>

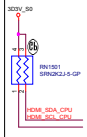
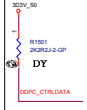
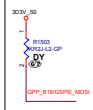
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

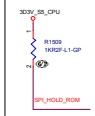
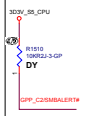
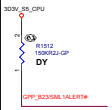
Title: CPU_POWER3

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Thursday, January 11, 2018 | Sheet 14 of 106

SSID = STRAP

Description	Display Port B Detected	Display Port C Detected	Reserved	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	Display Port D Detected
GPIO	GPP_E19	GPP_E21	SPI0_MISO	GPP_B18	GPP_B22	HDA_SDO	GPP_E23
Schematic							
High	Detected	Detected	Detected	Enable	LPC	Disable	Detected
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	Not Detected
	internal pull-down	internal pull-down	internal pull-up	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	Reserved	Reserved	Reserved	TLS Confi-dentiality	eSPI or LPC	Reserved
GPIO	GPP_B14	SPI0_MOSI	SPI0_IO2	SPI0_IO3	GPP_C2	GPP_C5	GPP_B23
Schematic							
High	Enable				Enable	eSPI	
Low	Disable				Disable	LPC	
	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-down	internal pull-down	internal pull-down

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Name	Internal Pull-up/ Pull-Down (Note 1)	De-Glitch (Note 2) Input	De-Glitch (Note 2) Output	Multiplexed With	Default	NMI or SMI Capable	Note
GPP_B22	20K PD (see note)	No	No	GSPI1_MOSI	GPO	None	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts
GPP_B23	20K PD (see note)	Yes	No	SML1ALERT#/ PCHHOT#	GPO	NMI SMI	• Also used as a strap. • The pull-down resistor is disabled after PLTRST# de-asserts

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
HD Audio Interface					
HDA_RST#	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SYNC	Primary	Internal Pull-down	Driven Low	Internal Pull-down	OFF
HDA_BLK	Primary	Driven Low	Driven Low	Driven Low	OFF
HDA_SDO	Primary	Internal Pull-down	Driven Low		OFF
HDA_SDI[1:0]	Primary	Internal Pull-down	Internal Pull-down		OFF

I/O Signal Planes and States

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
SPI0_CLK	Primary	Driven Low (See Note 1)	Driven Low	Driven Low	Off
SPI0_MOSI	Primary	Internal Pull up/ Pull-down (See Note 1 &2)	Driven Low	Driven Low	Off
SPI0_MISO	Primary	Internal Pull-up	Internal Pull-up	Internal Pull-up	Off
SPI0_CS0#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_CS1#	Primary	Internal Pull-up (See Note 1)	Driven High	Driven High	Off
SPI0_CS2#	Primary	Driven High (See Note 1)	Driven High	Driven High	Off
SPI0_IO[2:3]	Primary	Internal Pull-up (See Note 1)	Internal Pull-up	Internal Pull-up	Off
SPI1_CLK	Primary	Undriven	Undriven	Undriven	Off
SPI1_MOSI	Primary	Undriven	Undriven	Undriven	Off
SPI1_MISO	Primary	Undriven	Undriven	Undriven	Off
SPI1_CS#	Primary	Undriven	Undriven	Undriven	Off
SPI_IO[2:3]	Primary	Undriven	Undriven	Undriven	Off

Notes:
1. Pins are tri-stated (with weak internal pull-up) prior to RSMRST# de-assertion.
2. Weak internal pull-up resistor is enabled when RSMRST# is asserted and is switched to a weak internal pull-down when RSMRST# is de-asserted.

DDPB_CTRLDATA / GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. Bit 10 — Boot BIOS Destination 0 — SPI 1 — LPC *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_E23	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A19) as selected in Top Swap Block size soft strap (handled through FITC). *Notes:* 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. *Notes:* 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

<Case Design>
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: (Reserved)_SODIMM_SODIMM4
Size: Custom | Document Number: Strongbow_KL | Rev: 1
Date: Monday, January 15, 2018 | Sheet 15 of 108

Main Func = PCH

GPU

[76] GFX_PCIE_RX_P3
[76] GFX_PCIE_RX_N3
[76] GFX_PCIE_RX_P2
[76] GFX_PCIE_RX_N2
[76] GFX_PCIE_RX_P1
[76] GFX_PCIE_RX_N1
[76] GFX_PCIE_RX_P0
[76] GFX_PCIE_RX_N0
[76] GFX_PCIE_TX_CON_P3
[76] GFX_PCIE_TX_CON_N3
[76] GFX_PCIE_TX_CON_P2
[76] GFX_PCIE_TX_CON_N2
[76] GFX_PCIE_TX_CON_P1
[76] GFX_PCIE_TX_CON_N1
[76] GFX_PCIE_TX_CON_P0
[76] GFX_PCIE_TX_CON_N0

M.2 PCIE SSD1

[63] SSD1_PCIE_RX_N3
[63] SSD1_PCIE_RX_P3
[63] SSD1_PCIE_TX_N3
[63] SSD1_PCIE_TX_P3
[63] SSD1_PCIE_RX_N2
[63] SSD1_PCIE_RX_P2
[63] SSD1_PCIE_TX_N2
[63] SSD1_PCIE_TX_P2
[63] SSD1_PCIE_RX_N1
[63] SSD1_PCIE_RX_P1
[63] SSD1_PCIE_TX_N1
[63] SSD1_PCIE_TX_P1
[63] SSD1_PCIE_RX_N0
[63] SSD1_PCIE_RX_P0
[63] SSD1_PCIE_TX_N0
[63] SSD1_PCIE_TX_P0

HDD

[60] HDD_SATA_TX_P
[60] HDD_SATA_TX_N
[60] HDD_SATA_RX_P
[60] HDD_SATA_RX_N

WLAN

[61,89] WLAN_PCIE_RX_N
[61,89] WLAN_PCIE_RX_P
[61,89] WLAN_PCIE_TX_N
[61,89] WLAN_PCIE_TX_P

USB3 port1

[35] USB1_USB30_RX_N
[35] USB1_USB30_RX_P
[35] USB1_USB30_TX_N
[35] USB1_USB30_TX_P
[36] USB1_USB20_N
[36] USB1_USB20_P

USB3 port2

[35] USB2_USB30_RX_N
[35] USB2_USB30_RX_P
[35] USB2_USB30_TX_N
[35] USB2_USB30_TX_P
[35] USB2_USB20_N
[35] USB2_USB20_P

TYPE-C

[73] USB3_USB30_RX_N0
[73] USB3_USB30_RX_P0
[73] USB3_USB30_TX_N0
[73] USB3_USB30_TX_P0
[73] USB3_USB30_RX_N1
[73] USB3_USB30_RX_P1
[73] USB3_USB30_TX_N1
[73] USB3_USB30_TX_P1
[73] USB3_USB20_N
[73] USB3_USB20_P

[55] TS_USB20_N
[55] TS_USB20_P
[66,89] USB4_USB20_N
[66,89] USB4_USB20_P
[66,89] CR_USB20_N
[66,89] CR_USB20_P
[61,89] BT_USB20_N
[61,89] BT_USB20_P
[55] CCD_USB20_N
[55] CCD_USB20_P
[66,89] FP_USB20_N
[66,89] FP_USB20_P
[63] SSD1_PEDET
[63] DEVSLP2

DIS

WLAN

HDD

M.2 PCIE SSD1

M.2 PCIE SSD1

MLCCs on P63

3D3V_S0

R1601 10KR2F-L1-GP

PIRQA#

Layout Note:
1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

R1603 100R2F-L3-GP

PEG_RCOMPN_CPU
PEG_RCOMPP_CPU

CPU1H

SKYLAKE_ULT

PCIE/USB3/SATA

SSIC / USB3

USB2

USB1(USB 3.0)

USB2(USB 3.0)

USB3(Type-C)

USB3(Type-C)

USB1(USB 2.0)
USB2(USB 2.0)

TYPEC

SMALL BOARD(USB2.0)

BT

Touch Panel

CCD

Card Read
FP

RN1601 SRN1KJ-7-GP

RN1602 SRN10KJ-12-GP

R1602 113R2F-GP

R1604 10KR2F-L1-GP

USB_OC#

3D3V_S5_CPU

DY C1611 SCD1U25KX-L-GP

071.SKYLA.000U

CPU

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

M.2 auto detection

Q1602 2N7002K-2-GP

84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.27002.0N31

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

	KBL Premium U		Acer 2015		2017 R15(Premium)		2017 R15(base)
Lane1	USB3 Port1		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane2	USB3 Port2		USB 3 (I/O)		USB 3 (I/O)		USB 3 (I/O)
Lane3	USB3 Port3		USB 3 (I/O)		USB 3 Type-C (I/O)		USB 3 Type-C (I/O)
Lane4	USB3 Port4						
Lane5	USB3 Port5 (Premium)	PCIe Port1	dGPU		dGPU		dGPU
Lane6	USB3 Port6 (Premium)	PCIe Port2					
Lane7		PCIe Port3					
Lane8		PCIe Port4					
Lane9		PCIe Port5	LAN				
Lane10		PCIe Port6	WIFI		WIFI		WIFI
Lane11	SATA0 (Base/Premium)	PCIe Port7 (Premium)	HDD		HDD		HDD
Lane12	SATA1 (Base/Premium)	PCIe Port8 (Premium)	ODD				
Lane13		PCIe Port9					
Lane14		PCIe Port10	NA	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal	M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal		M.2 SSD (PCIe x4) * BIOS needs to set PCIe x4 lane reversal
Lane15	SATA1 (Premium)	PCIe Port11					
Lane16	SATA2 (Premium)	PCIe Port12	M.2 SSD (SATA x1)		M.2 SSD SATA		
	USB2 Port1		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port2		USB 3 (I/O)		USB 3 (I/O) (USB20)		USB 3 (I/O) (USB20)
	USB2 Port3		USB 3 (I/O)		USB 2 Type-C (I/O)		USB 2 Type-C (I/O)
	USB2 Port4		USB 2 (I/O) / SensorHub		USB 2 (I/O)		USB 2 (I/O)
	USB2 Port5		BT		BT		BT
	USB2 Port6		TS		TS		TS
	USB2 Port7		CCD		CCD		CCD
	USB2 Port8		CR (USB) / FP		CR		CR
	USB2 Port9		FG		FP		FP
	USB2 Port10						

CPU1I

SKYLAKE_ULT

CSI-2

EMMC

GPP_F: VCCPGPPF = 1.8V Only

1.8V Only

CPU

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(PCIE/SATA/USB)

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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Main Func = PCH

DIS

[76] PEG_CLK_CPU_P
[76] PEG_CLK_CPU_N
[76] PEG_CLKREQ_CPU#

WLAN

[61,89] WLAN_CLK_CPU_N
[61,89] WLAN_CLK_CPU_P
[61,89] WLAN_CLKREQ_CPU#

NGFF1

[63] SSD1_CLK_CPU_N
[63] SSD1_CLK_CPU_P
[63] SSD1_CLKREQ_CPU_N

KBC

[24] RTCRST_ON

CPU1J — 10 OF 20 — CLOCK SIGNALS — SKYLAKE_ULT

DIS
PEG_CLK_CPU_N — D42 — CLKOUT_PCIE_N0
PEG_CLK_CPU_P — C42 — CLKOUT_PCIE_P0
PEG_CLKREQ_CPU# — AR10 — GPP_B5/SRCCLKREQ0#

LAN_CLKREQ_CPU# — B42 — CLKOUT_PCIE_N1
A42 — CLKOUT_PCIE_P1
AT7 — GPP_B6/SRCCLKREQ1#

WLAN
WLAN_CLK_CPU_N — D41 — CLKOUT_PCIE_N2
WLAN_CLK_CPU_P — C41 — CLKOUT_PCIE_P2
WLAN_CLKREQ_CPU# — AT8 — GPP_B7/SRCCLKREQ2#

NGFF1
SSD1_CLK_CPU_N — D40 — CLKOUT_PCIE_N3
SSD1_CLK_CPU_P — C40 — CLKOUT_PCIE_P3
SSD1_CLKREQ_CPU_N — AT10 — GPP_B8/SRCCLKREQ3#

SSD2_CLKREQ_CPU_N# — B40 — CLKOUT_PCIE_N4
A40 — CLKOUT_PCIE_P4
AU8 — GPP_B9/SRCCLKREQ4#

E40 — CLKOUT_PCIE_N5
E38 — CLKOUT_PCIE_P5
SRCCLKREQ5# — AU7 — GPP_B10/SRCCLKREQ5#

CPU

CLKOUT_ITPXDP_N — F43
CLKOUT_ITPXDP_P — E43

GPD8/SUSCLK — BA17 — SUS_CLK_CPU — 1 — TP1701

XTAL24_IN — E37 — XTL_24M_X1_CPU
XTAL24_OUT — E35 — XTL_24M_X2_CPU

1D0V_S5

XCLK_BIASREF — E42 — XCLK_BIASREF — R1701 2K7R2F-GP

RTCX1 — AM18 — XTL_32K_X1_CPU
RTCX2 — AM20 — XTL_32K_X2_CPU

SRTCRST# — AN18 — SRTC_RST#
RTCRST# — AM16 — RTC_RST#

3D3V_RTC_AUX

RN1701 SRN20KJ-1-GP

RTC Reset

C1702 SC1U50V3KX-GP
G1701 GAP-OPEN
C1701 SC1U50V3KX-GP

SKYLAKE-U-GP

For AFR

RTCRST_ON — G — Q1701 — D — RTC_RST#
RTC_RST#_R — S
2N7002K-2-GP

R1703 100KR2F-L3-GP
R1704 2K2R2J-L1-GP

84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.27002.0N31

XTL_32K_X1_CPU
XTL_32K_X2_CPU
R1702 10MR2J-L-GP
X1701 XTAL-32D768KHZ-88-GP
082.30003.0191
C1703 SC15P50V2JN-2-GP
C1704 SC15P50V2JN-2-GP

XTL_24M_X1_CPU
C1705 SC18P50V2JN-1-GP
U22
R1705 1MR2F-L-GP
INPUT/OUTPUT#1
NC#2
INPUT/OUTPUT#3
X1702 XTAL-24MHZ-135-GP
082.30006.0041
2nd = 82.30004.A01
XTL_24M_X2_CPU
U22
C1706 SC18P50V2JN-1-GP
U22

close to CPU

3D3V_S0
SSD1_CLKREQ_CPU_N
PEG_CLKREQ_CPU#
WLAN_CLKREQ_CPU#
SSD2_CLKREQ_CPU_N
RN1702 SRN10KJ-12-GP
LAN_CLKREQ_CPU#
SRCCLKREQ5#
RN1703 SRN10KJ-L-GP

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: MCP_CLOCK
Size: Custom
Document Number: Strongbow_KL
Rev: 1
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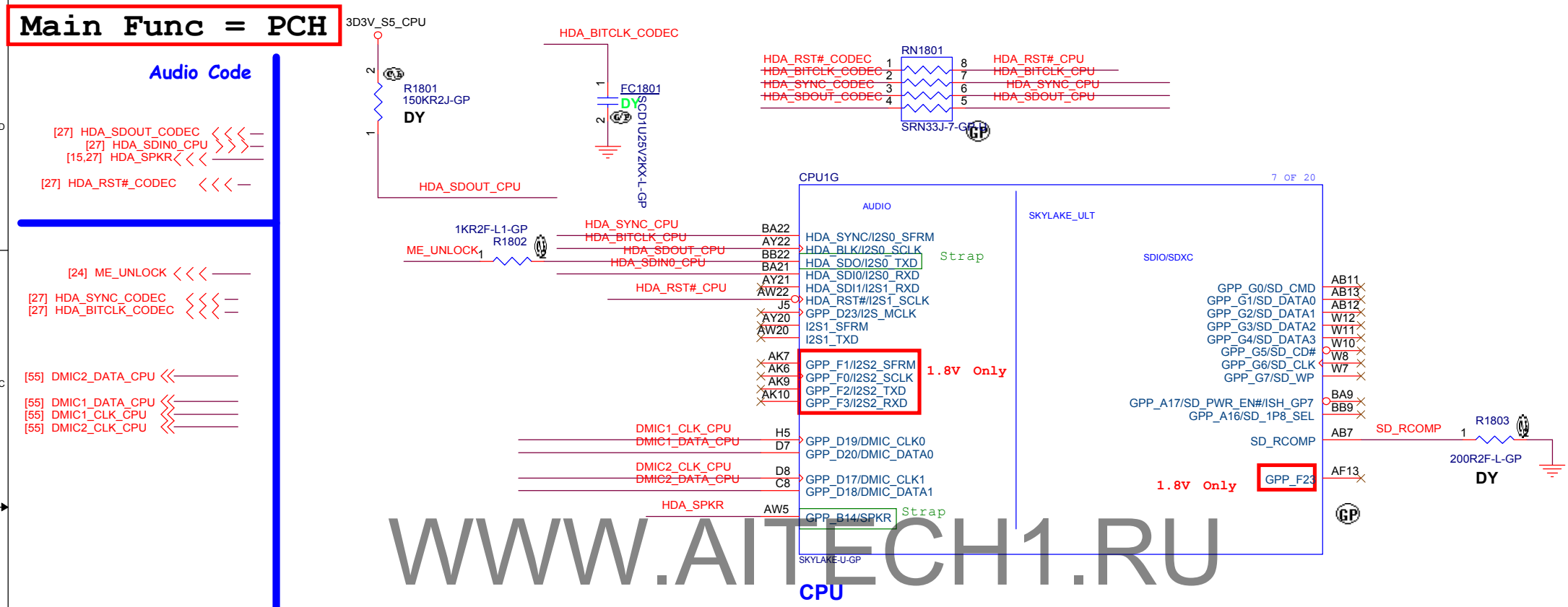

18.3 Terminating Unused SDXC Signals

SDXC signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDXC interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

Additionally, if SDXC interface is not used, the SD_RCOMP pin does not need to be connected to a RCOMP resistor.

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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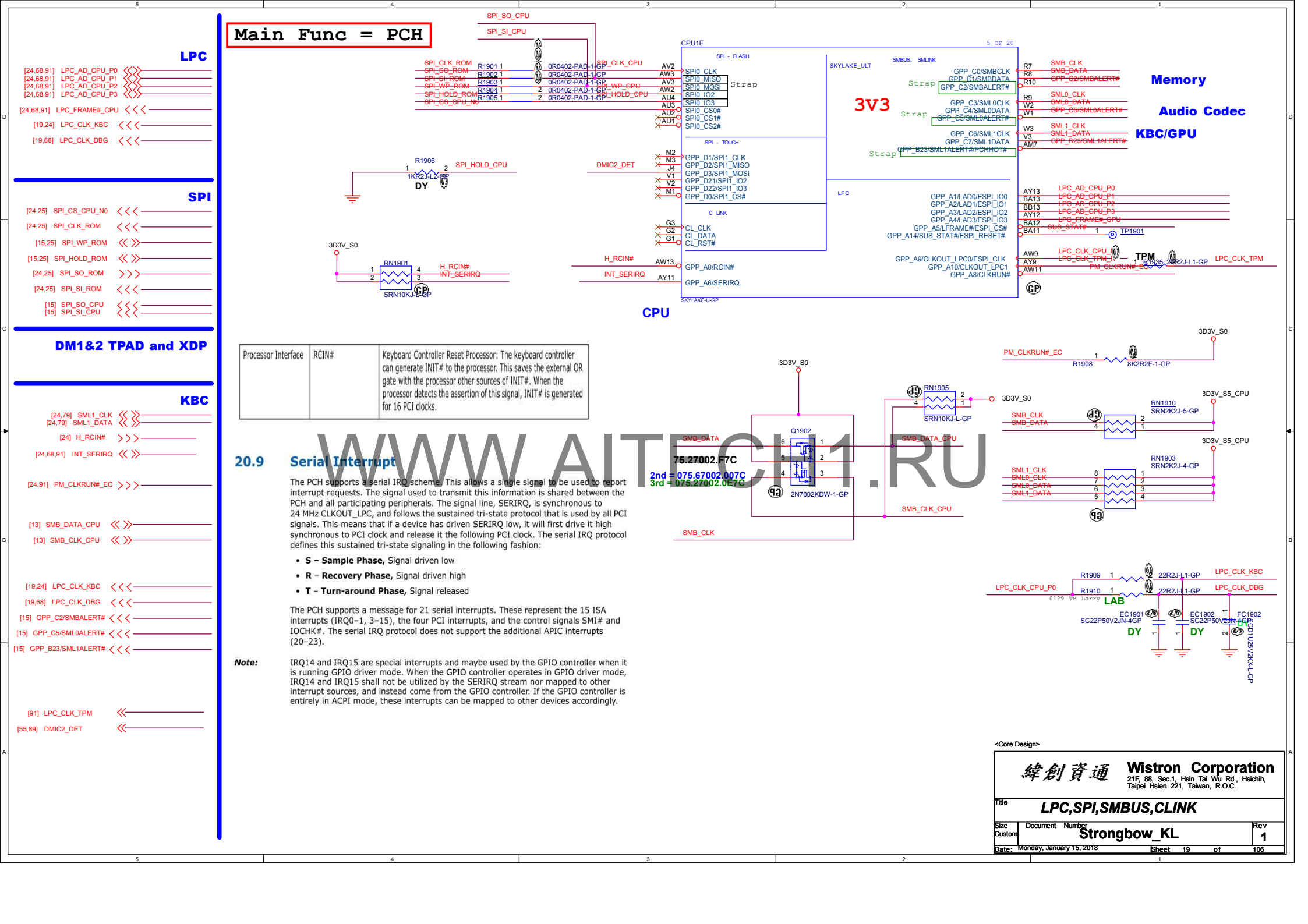

Processor Interface	RCIN#	Keyboard Controller Reset Processor: The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the processor other sources of INIT#. When the processor detects the assertion of this signal, INIT# is generated for 16 PCI clocks.

20.9 Serial Interrupt

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to PCI clock and release it the following PCI clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase,** Signal driven low
- **R – Recovery Phase,** Signal driven high
- **T – Turn-around Phase,** Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

Note: IRQ14 and IRQ15 are special interrupts and maybe used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

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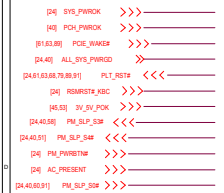
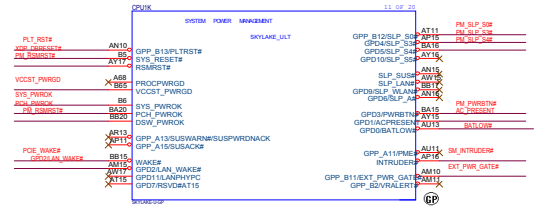
Title: LPC,SPI,SMBUS,CLINK

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 19 of 106

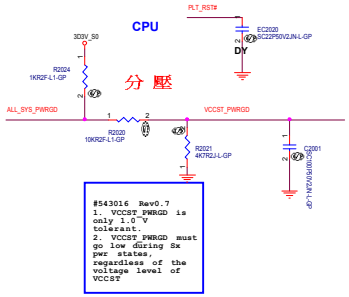
Main Func = PCH

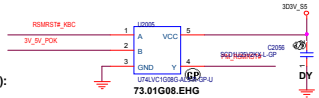




BATLOW#:
Pull-up required even if not implemented.

CPU



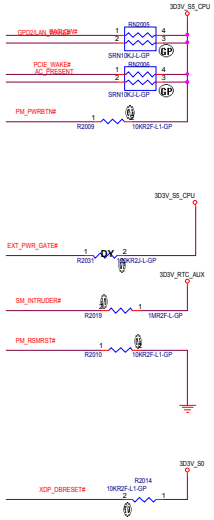


GPP_A13-15 pin(LPC/eSPI):

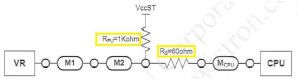
73.01G08.EHG

2nd = 73.01G08.DHG

Name	Internal Pull-Up/ Pull-Down (Note 1)	De-Glitch (Note 2)		Multiplexed With	Default
		Input	Output		
GPP_A13	None	No	Yes	LPC mode: SUSWARN#/ SUSPWRDNACK eSPI mode: None	SUSWANRN#/ SUSPWRDNACK (LPC mode) GPI (eSPI mode)
GPP_A14	None	No	Yes	LPC mode: SUS_STAT# eSPI mode: ESPI_RESET#	SUS_STAT# (LPC mode) ESPI_RESET# (eSPI mode)
GPP_A15	None	No	Yes	LPC mode: SUS_ACK# eSPI mode: None	SUS_ACK# (LPC mode) GPI (eSPI mode)



VCCST_PWRGOOD



- VCCST_PWRGOOD is a signal on the processor that indicates both the VCCST power supply and VDDQ power supply are within voltage tolerance specification

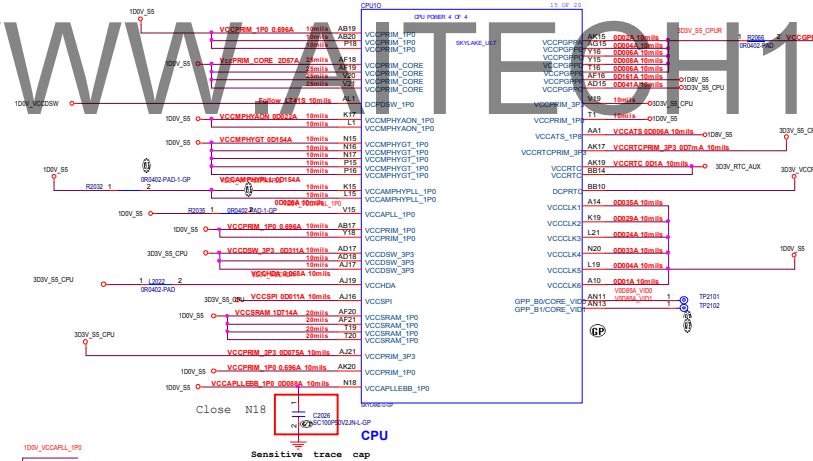


Table 2: eSPI/LPC Pinlist for SKL-PCH

SKL-PCH Pin Name	Direction	LPC Signal	eSPI Signal	Pin Description
GPP_A_0	in	RCINB	<GPIO>	
GPP_A_1	inout	LAD_0	ESPI_IO_[0]	LPC Cmd/Addr/Data or eSPI Data [0]
GPP_A_2	inout	LAD_1	ESPI_IO_[1]	LPC Cmd/Addr/Data or eSPI Data [1]
GPP_A_3	inout	LAD_2	ESPI_IO_[2]	LPC Cmd/Addr/Data or eSPI Data [2]
GPP_A_4	inout	LAD_3	ESPI_IO_[3]	LPC Cmd/Addr/Data or eSPI Data [3]
GPP_A_5	out	LFRAMEB	ESPI_CSB	LPC Frame or eSPI Chip Select
GPP_A_6	inout	SERIRQ	<GPIO>	
GPP_A_7	iod	PIRQAB	<GPIO>	
GPP_A_9	out	LPC_CLKOUT_ 0	ESPI_CLK	
GPP_A_14	out	SUS_STATB	ESPI_RESETB	
GPP_C_5_SML0ALERTB	input	ESPI_EN Pin Strap		eSPI Enable Pin Strap; sampled at RMSRST# deassertion 0: LPC; 1: eSPI
VCCPGPPA	-	3.3V	1.8V	Voltage for all GPIOs in GPP_A group

NOTE: All pin mappings are subject to change. Refer to the SKL-PCH EDS for final pin list.

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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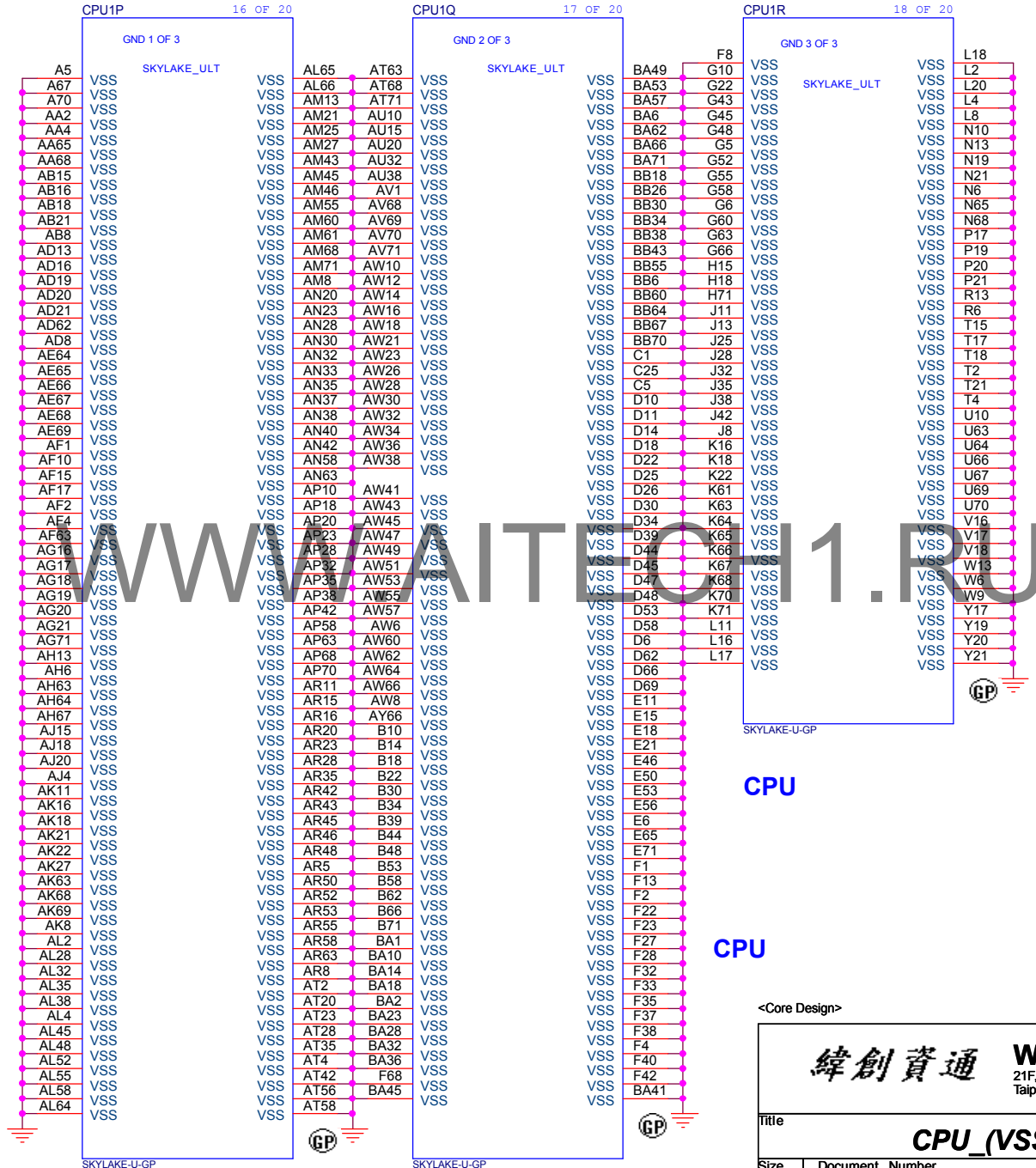
Main Func = PCH



<Core Design>

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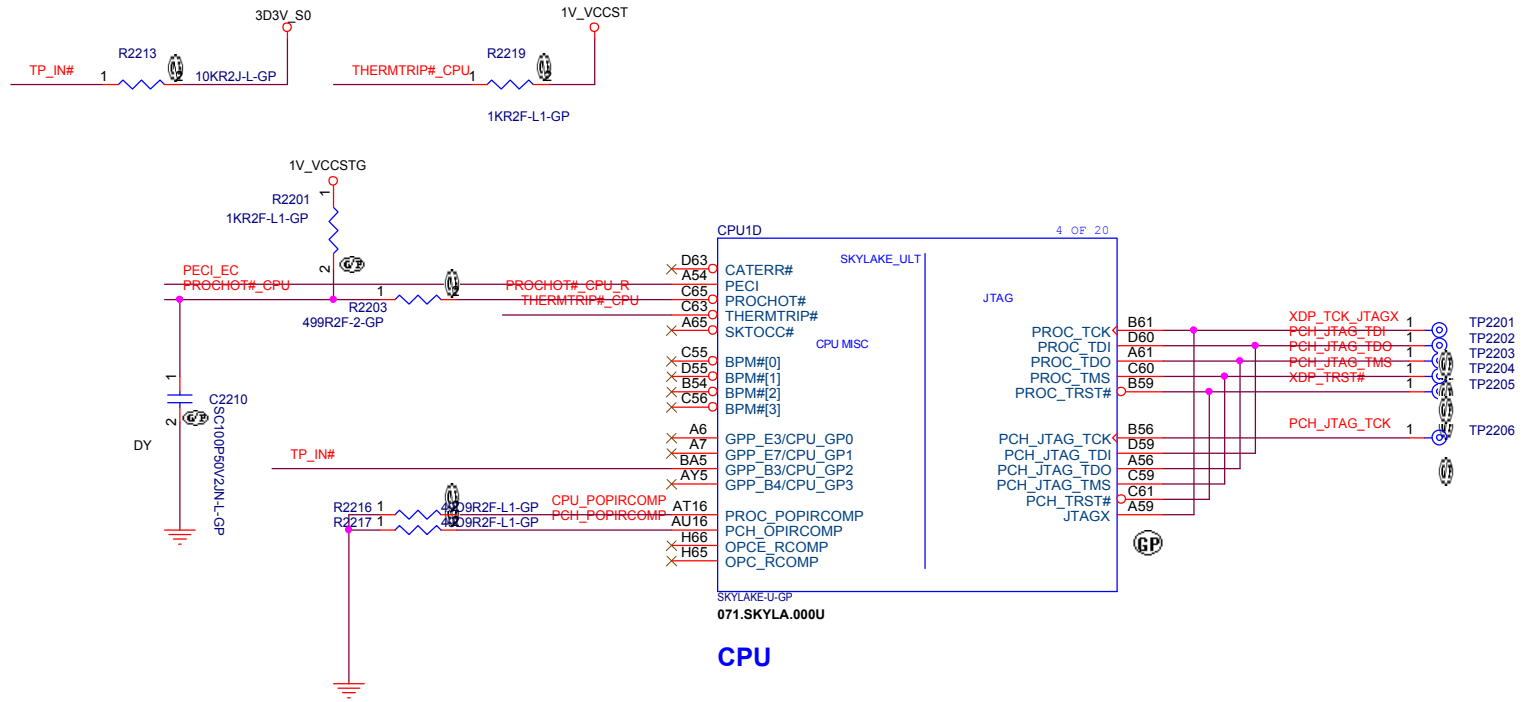
Title: *CPU_(VSS)*		
Size: Custom	Document Number: **Strongbow_KL**	Rev: 1
Date: Monday, January 15, 2018	Sheet 21 of 106	

Main Func = CPU

[24] PECI_EC
[24,44,46] PROCHOT#_CPU
[65] TP_IN#



CPU

PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All processor lines
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	OD	SE	All processor lines

<Core Design>

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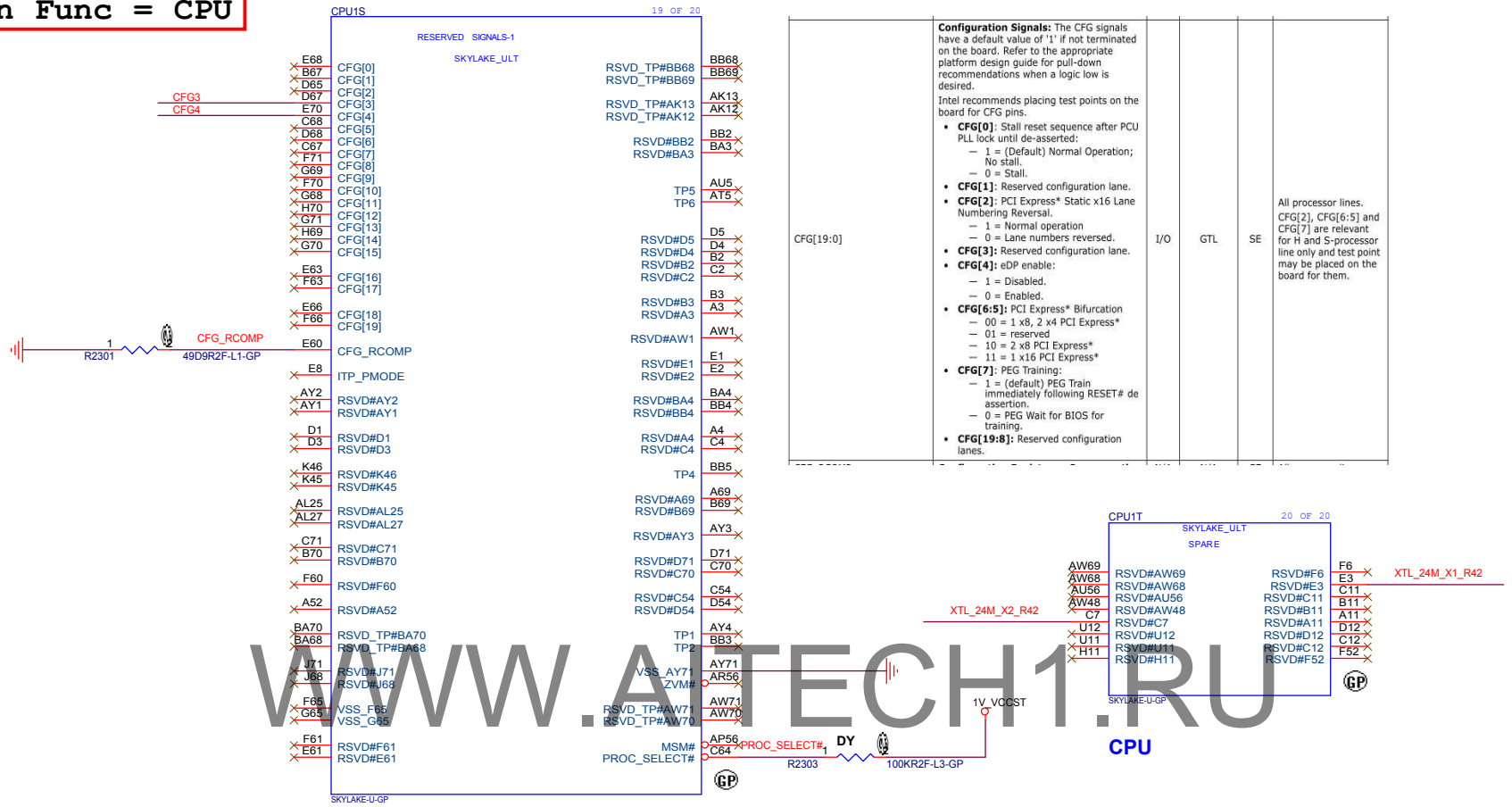
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(JTAG/CPU SIDE BAND)

Size: Custom | Document Number: Strongbow_KL | Rev: 1

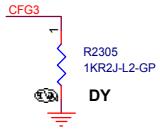
Date: Monday, January 15, 2018 | Sheet 22 of 106

Main Func = CPU

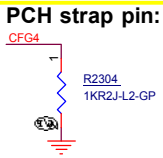


CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

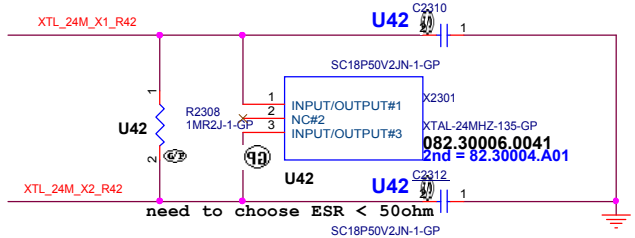
PCH strap pin:



PCH strap pin:



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port. 1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.



PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for SKL.			N/A	All processor lines

<Core Design>

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Title: **CPU_RESERVED,CFG**

Size: Custom | Document Number: **Strongbow_KL** | Rev: 1

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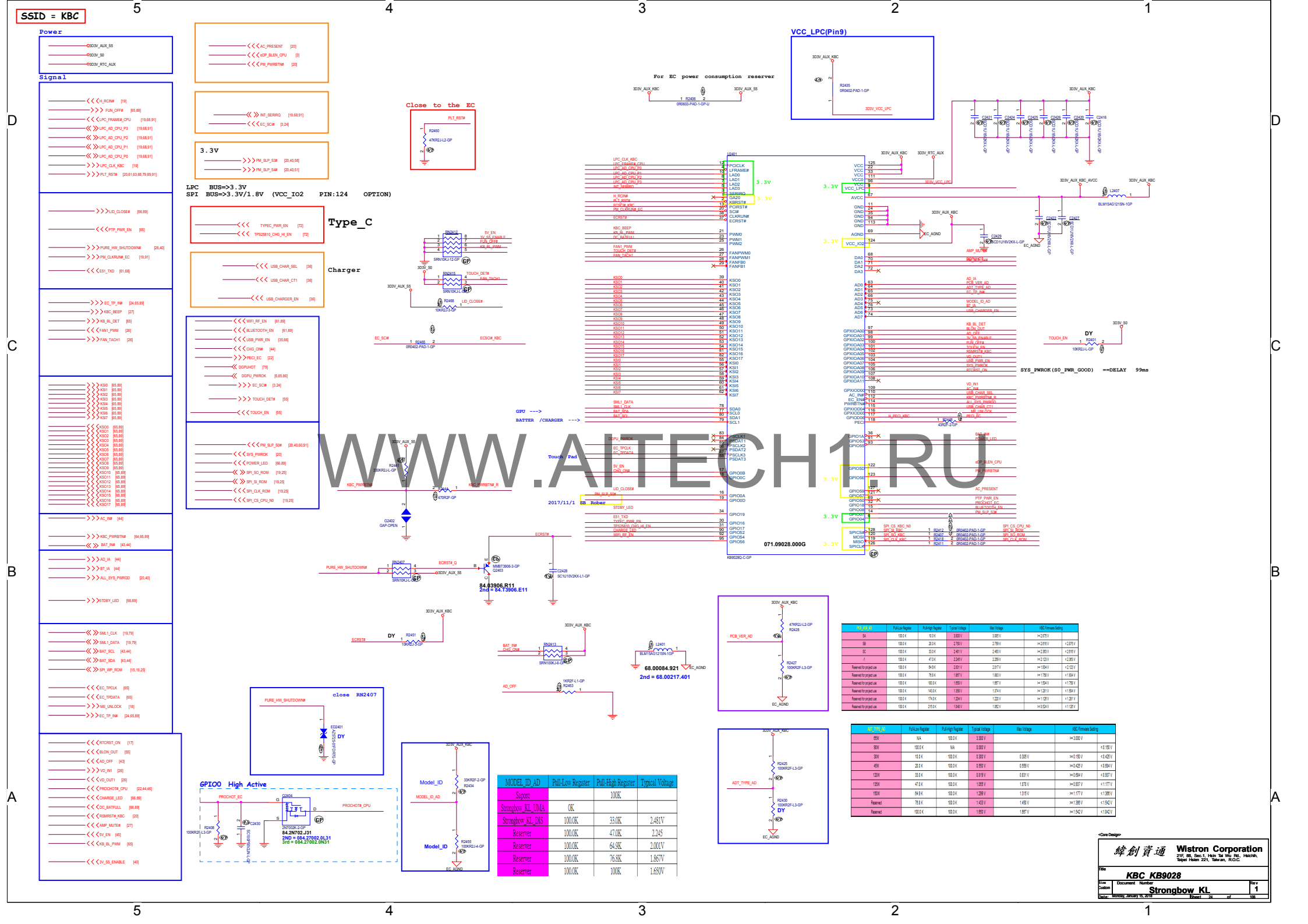


MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Sapero		100K	
Strongbow_KL_UMA	0K		
Strongbow_KL_DIS	100.0K	33.0K	2.481V
Reserver	100.0K	47.0K	2.245
Reserver	100.0K	64.9K	2.001V
Reserver	100.0K	76.8K	1.867V
Reserver	100.0K	100K	1.650V

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
0A	100.0 K	10.0 K	3.300 V	3.300 V	>= 2.675 V	
0B	100.0 K	20.0 K	3.150 V	>= 2.916 V	< 2.675 V	
0C	100.0 K	33.0 K	2.481 V	>= 2.301 V	< 2.916 V	
0	100.0 K	47.0 K	2.245 V	>= 2.123 V	< 2.301 V	
Reserved for project use	100.0 K	64.9 K	2.001 V	>= 1.894 V	< 2.123 V	
Reserved for project use	100.0 K	76.8 K	1.867 V	>= 1.769 V	< 1.894 V	
Reserved for project use	100.0 K	100.0 K	1.650 V	>= 1.554 V	< 1.769 V	
Reserved for project use	100.0 K	143.0 K	1.389 V	>= 1.291 V	< 1.554 V	
Reserved for project use	100.0 K	174.0 K	1.224 V	>= 1.129 V	< 1.291 V	
Reserved for project use	100.0 K	210.0 K	1.048 V	>= 0.924 V	< 1.129 V	

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	3.300 V		>= 3.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.335 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.553 V	0.659 V	>= 0.425 V	< 0.884 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.884 V	< 0.937 V
150W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
180W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.395 V
Reserved	76.8 K	100.0 K	1.433 V	1.458 V	>= 1.395 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

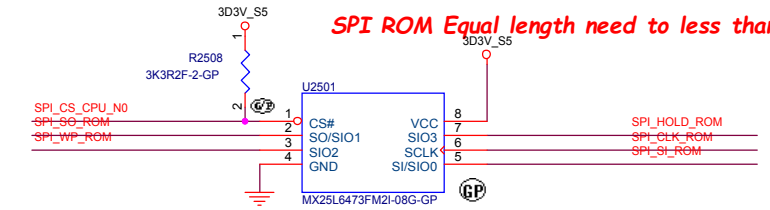
[19,24] SPI_CS_CPU_N0
[19,24] SPI_SO_ROM
[15,19] SPI_WP_ROM

[15,19] SPI_HOLD_ROM
[19,24] SPI_CLK_ROM
[19,24] SPI_SI_ROM
[6] RTC_DET#

Main Func = SPI Flash

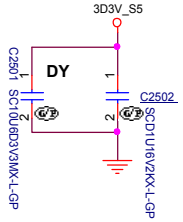
SPI FLASH ROM (8M byte) for PCH

SPI ROM Equal length need to less than 500mil

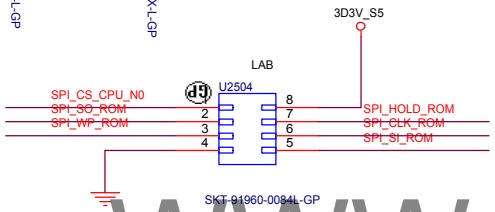


072.25647.000D

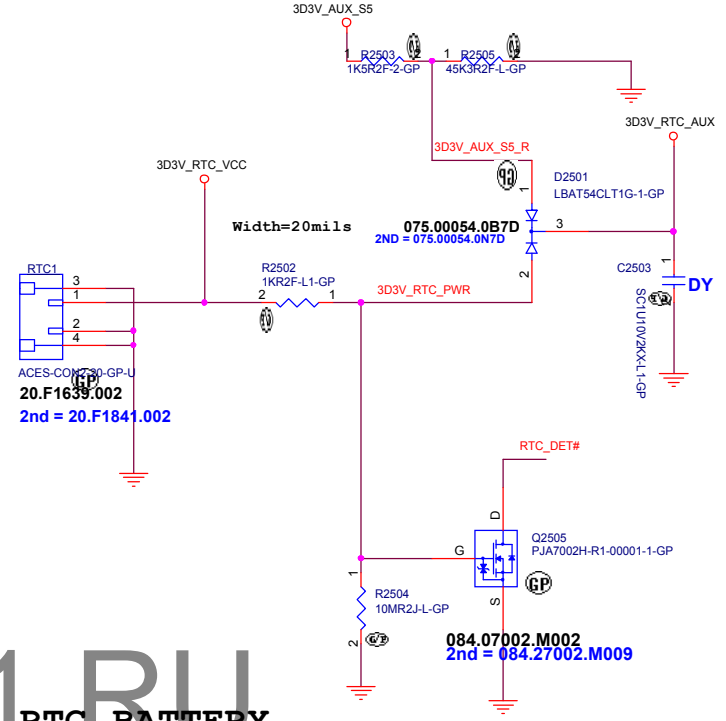
2nd = 072.25Q64.0H01



072.25647.000D_MX25L6473FM2I-08G_MXIC
072.25Q64.0H01_W25Q64FVSSIQ_WINBOND



Main Func = RTC



RTC BATTERY
1st= TBD
2nd= TBD

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

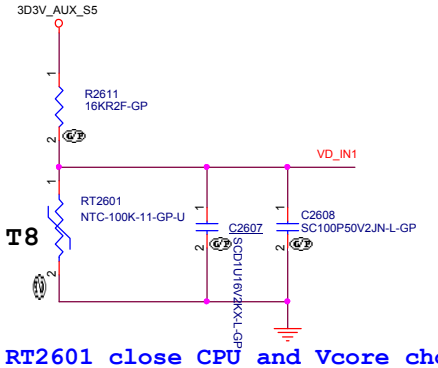
Title: ***Flash(KBC+PCH)/RTC***

Size: Custom | Document Number: **Strongbow_KL** | Rev: **1**

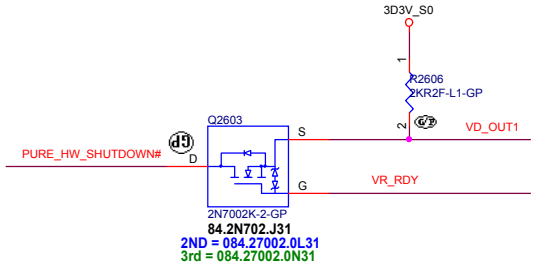
Date: Monday, January 15, 2018 | Sheet 25 of 106

SSID = Thermal

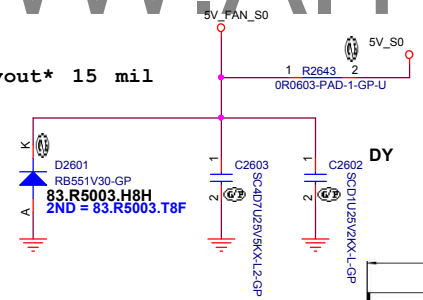
[24] VD_IN1
[24] FAN1_PWM
[24] FAN_TACH1
[24] FAN_TACH1_C
[24,40] PURE_HW_SHUTDOWN#
[24] VD_OUT1
[40,46] VR_RDY
[20,24,40,58] PM_SLP_S3#

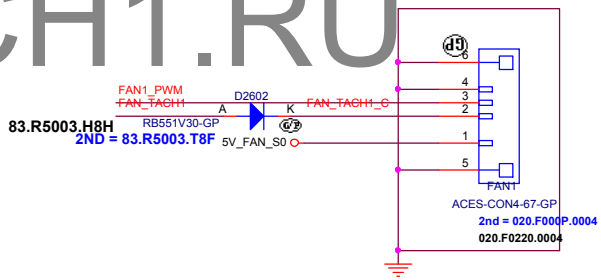


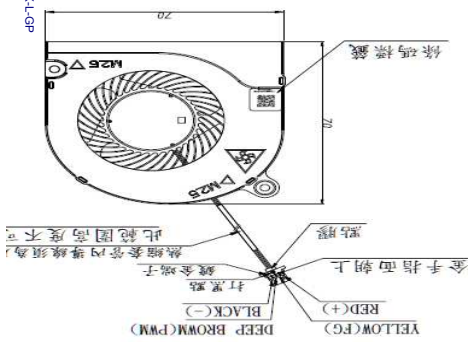
RT2601 close CPU and Vcore chock
VD_IN1 trace 10 mli



Layout 15 mil







<Core Design>

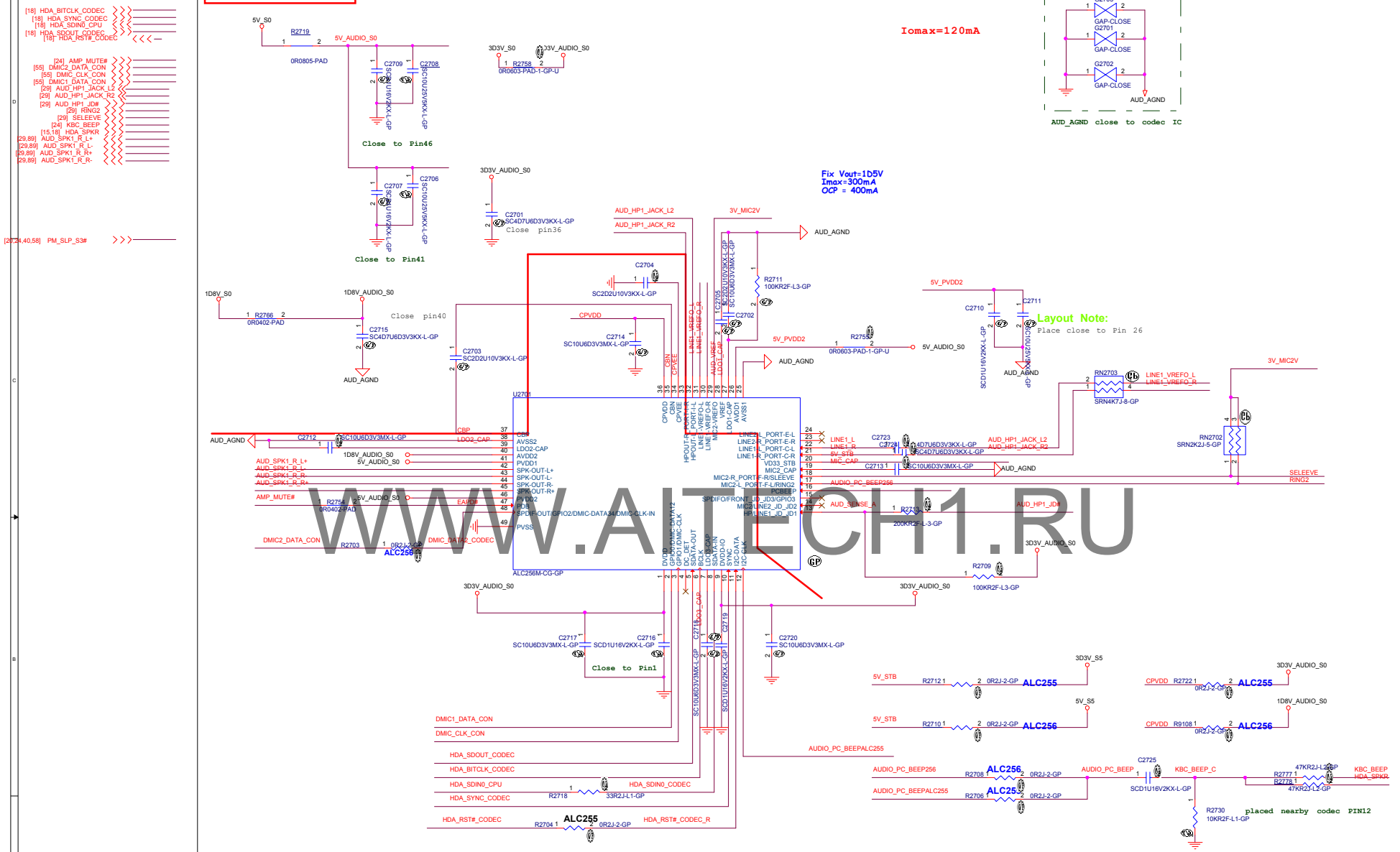
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793

Size	Document Number	Rev
Custom	Strongbow_KL	1

Date: Monday, January 15, 2018 Sheet 26 of 106

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC256

Size: Custom | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 27 of 106

Blanking

<Core Design>

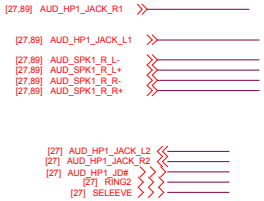
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

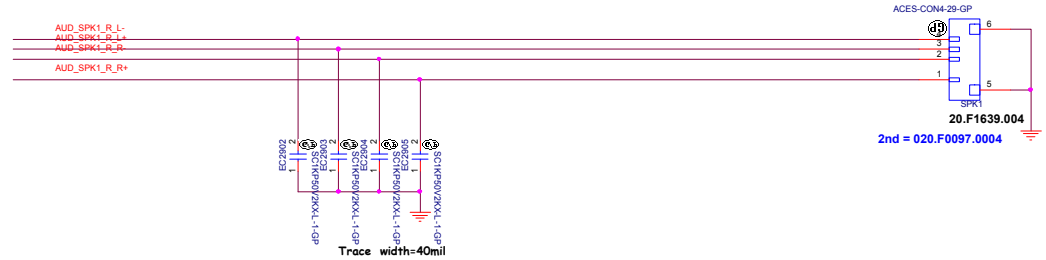
Title

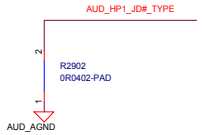
Size	Document Number	Rev
A4	Strongbow_KL	1

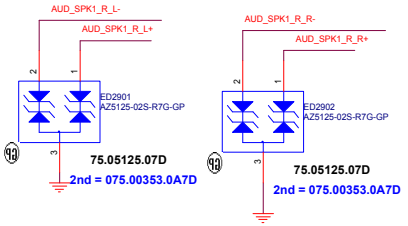
Date: Thursday, January 11, 2018 Sheet 28 of 106

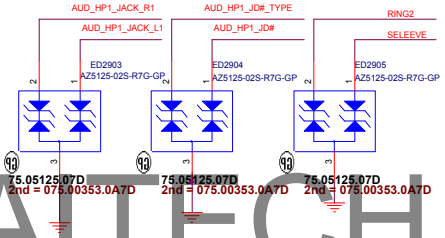
SSID = AUDIO *Speaker*

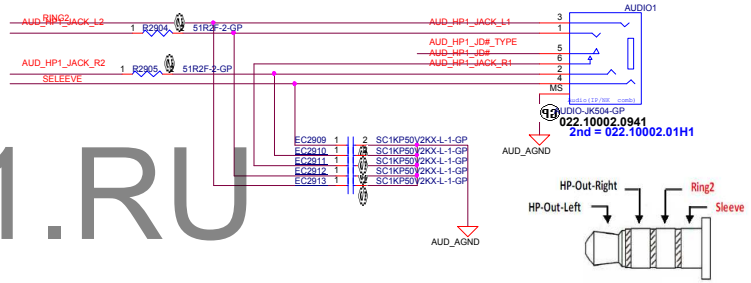












<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Speaker/HPMIC**

Size	Document Number	Rev
Custom	Strongbow_KL	1
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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	
Size: A4	Document Number: **Strongbow_KL**
Rev: 1	
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(LAN+VGA) CONNECTOR

Size	Document Number	Rev
A4	Strongbow_KL	1

Date: Thursday, January 11, 2018 Sheet 31 of 106

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RTS5170(CARD READER)*

Size	Document Number	Rev
A3	Strongbow_KL	1

Date: Thursday, January 11, 2018 Sheet 32 of 106

SSID = SDIO

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size	Document Number	Rev
A4	Strongbow_KL	1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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[16] USB1_USB20_N
[16] USB1_USB20_P
[24,66] USB_PWR_EN
[16] USB1_USB30_RX_N
[16] USB1_USB30_RX_P
[16] USB1_USB30_TX_N
[16] USB1_USB30_TX_P
[89] USB1_CON_USB20_N
[89] USB1_CON_USB20_P
[36] USB2_USB20_CHAR_N
[36] USB2_USB20_CHAR_P
[16] USB2_USB30_RX_N
[16] USB2_USB30_RX_P
[16] USB2_USB30_TX_N
[16] USB2_USB30_TX_P
[89] USB2_CON_USB20_N
[89] USB2_CON_USB20_P

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

EU3501
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
C3508 SCD1U16V2KX-L-GP
C3509 SCD1U16V2KX-L-GP
USB1
SKT-USB13-182-GP
C3504 SC100U6D3V6MX-GP
DLM0NSN900HY2D-GP EL3501
EU3503
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.PUSB3.0073
High Active 2A
U3501 G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
C3501 SC1U10V2KX-L-GP
C3502 SCD1U16V2KX-L-GP
EU3502
L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
C3520 SCD1U16V2KX-L-GP
C3521 SCD1U16V2KX-L-GP
USB2
SKT-USB13-182-GP
DLM0NSN900HY2D-GP EL3502
C3516 SC100U6D3V6MX-GP
EC3501 SCD1U16V2KX-L-GP

緯創資通 Wistron Corporation
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Title: USB 3.0
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[24] USB_CHARGER_EN

[24] USB_CHAR_SEL

[24] USB_CHAR_CT1

To Connector

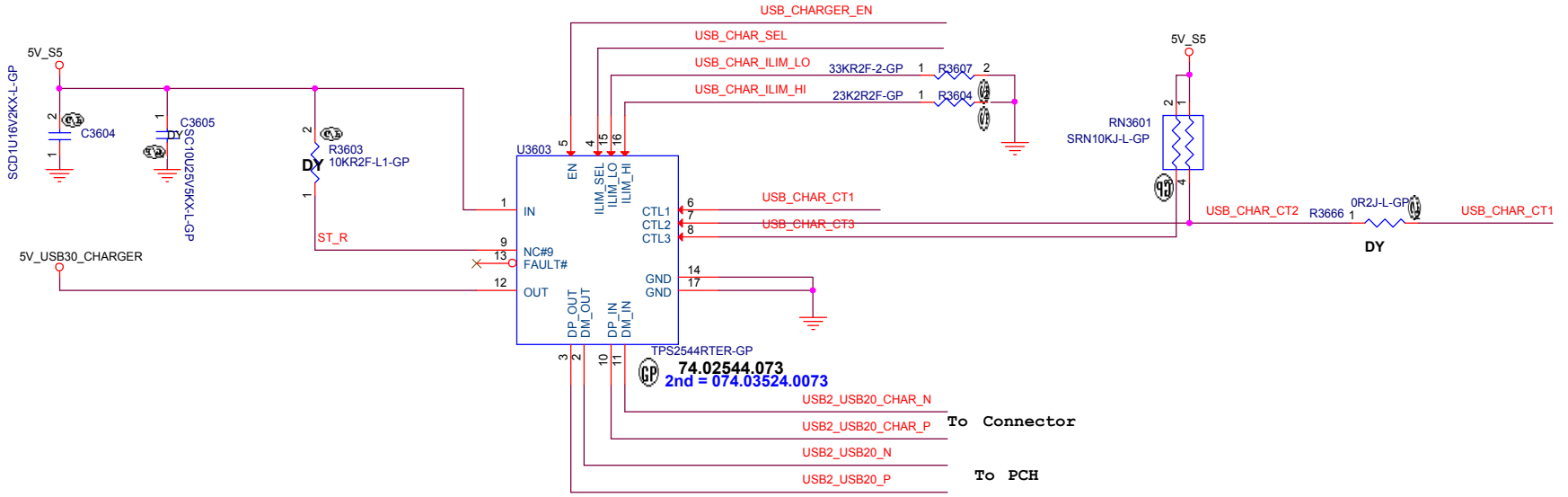
[35] USB2_USB20_CHAR_N

[35] USB2_USB20_CHAR_P

To PCH

[16] USB2_USB20_N

[16] USB2_USB20_P



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP Auto	ILIM_HI	Data Lines Disconnected
0	0	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

S5 (at low bateery and non support charger)

S3 and S5 state

S0 and S3 (at low bateery and non support charger)

S0 state

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Strongbow_KL	1

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<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	
Size: A4	Document Number: **Strongbow_KL** — Rev: 1
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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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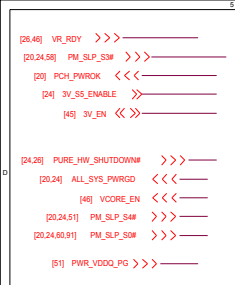
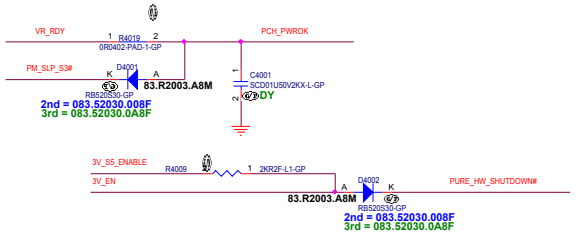
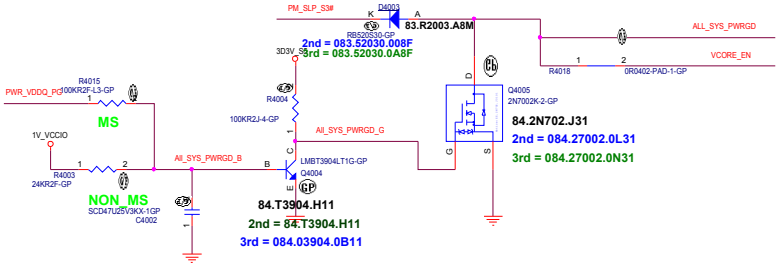
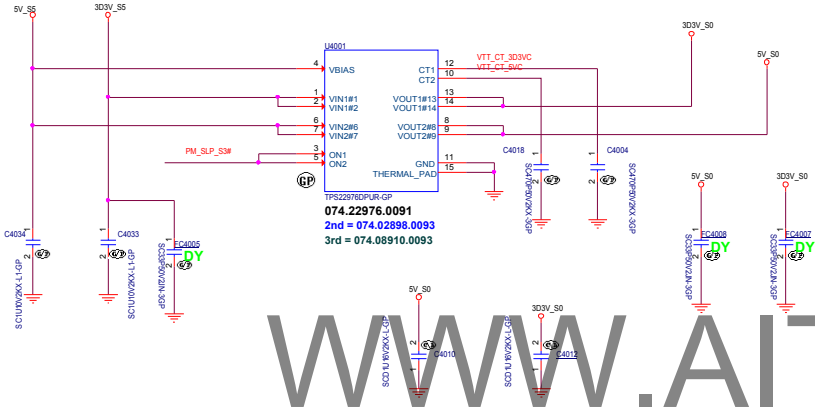
Power Sequence

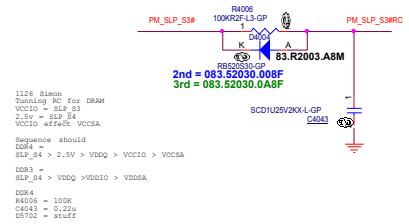


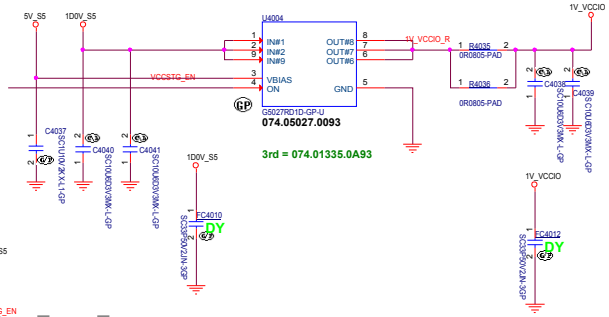


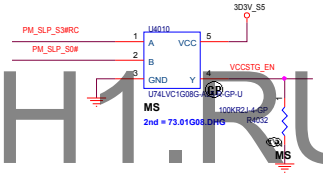


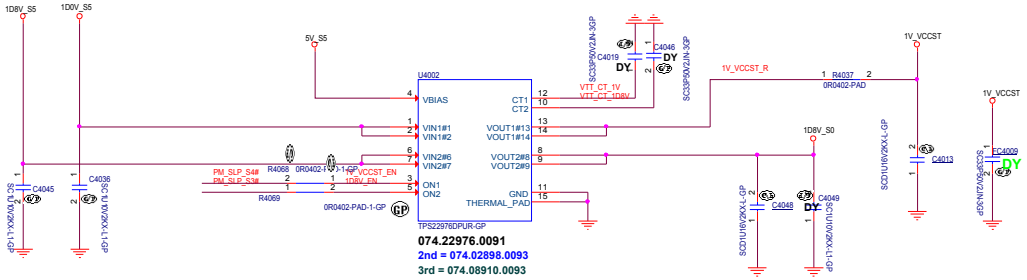
ANNIE Run Power











<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DCIN JACK

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ANNIE solution

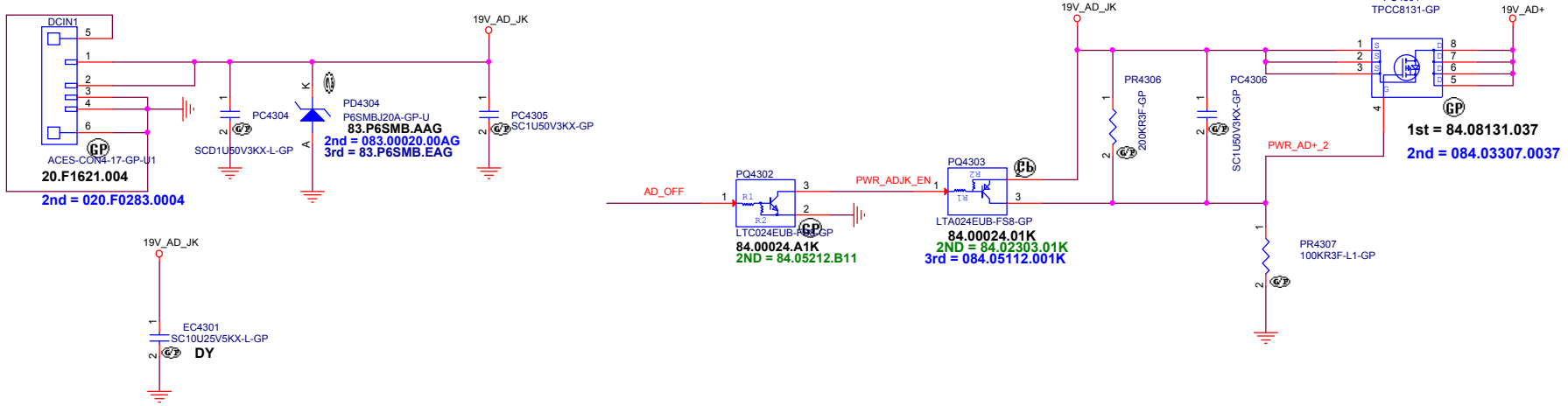
[24] AD_OFF

[24,44] BAT_IN#
[24,44] BAT_SCL
[24,44] BAT_SDA

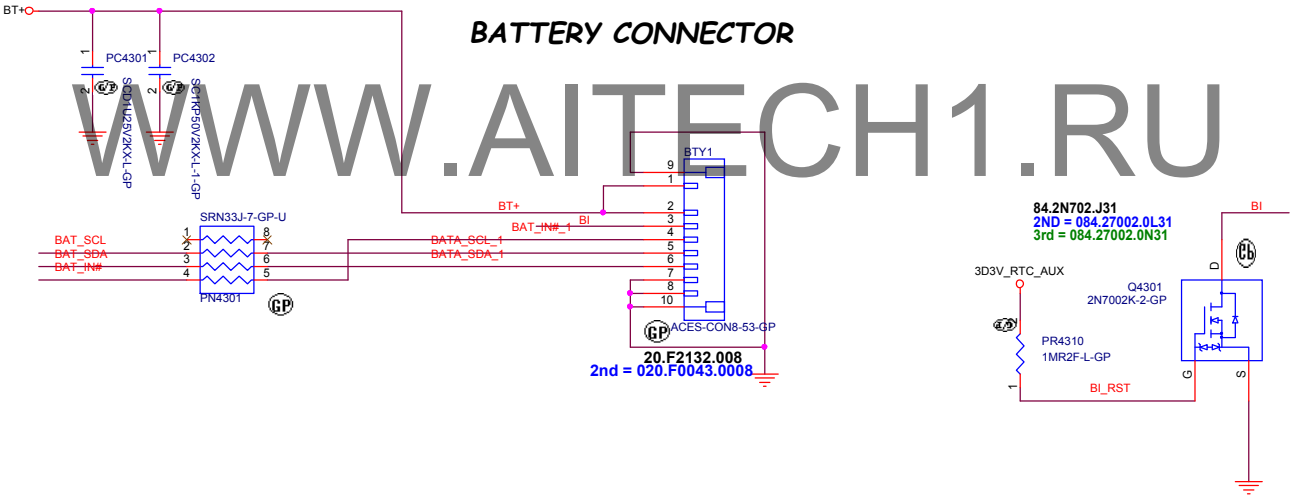
[89] BI
[89] BAT_IN#_1
[89] BATA_SCL_1
[89] BATA_SDA_1

[66,89] BI_RST

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

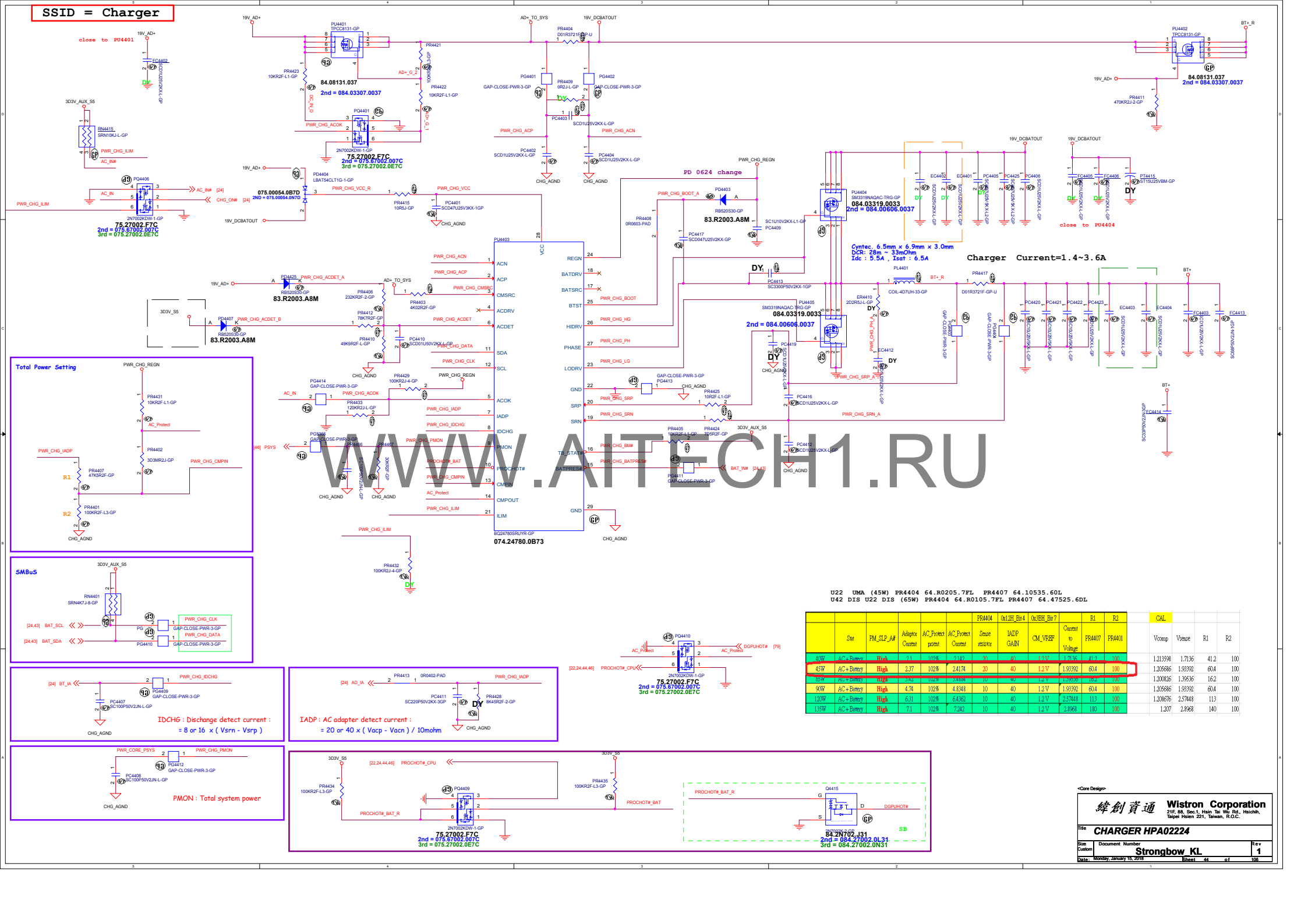
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size: A3 | Document Number: Strongbow_KL | Rev: 1

Date: Monday, January 15, 2018 | Sheet 43 of 106

SSID = Charger



U22 UMA (45W) PR4404 64.R0205.7FL PR4407 64.10535.60L
U42 DIS U22 DIS (65W) PR4404 64.R0105.7FL PR4407 64.47525.6DL

	Stat	PM_SLP_A#	Adaptor Current	AC_Protect prcent	AC_Protect Current	PR4404 Sense resistor	0x12H_Bit4 IADP GAIN	0x3BH_Bit 7 OM_VREF	Current to Voltage	R1 PR4407	R2 PR4401	CAL Vcomp	Vsense	R1	R2
40W	AC+Battery	High	2.1	102%	2.142	20	40	1.2 V	1.71396	41.2	100	1.213598	1.71396	41.2	100
45W	AC+Battery	High	2.37	102%	2.4174	20	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
65W	AC+Battery	High	3.42	102%	3.4884	10	40	1.2 V	1.39536	16.2	100	1.200826	1.39536	16.2	100
90W	AC+Battery	High	4.74	102%	4.8348	10	40	1.2 V	1.93392	60.4	100	1.205686	1.93392	60.4	100
120W	AC+Battery	High	6.31	102%	6.4362	10	40	1.2 V	2.57448	113	100	1.208676	2.57448	113	100
135W	AC+Battery	High	7.1	102%	7.242	10	40	1.2 V	2.8968	180	100	1.207	2.8968	140	100

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER HPA02224

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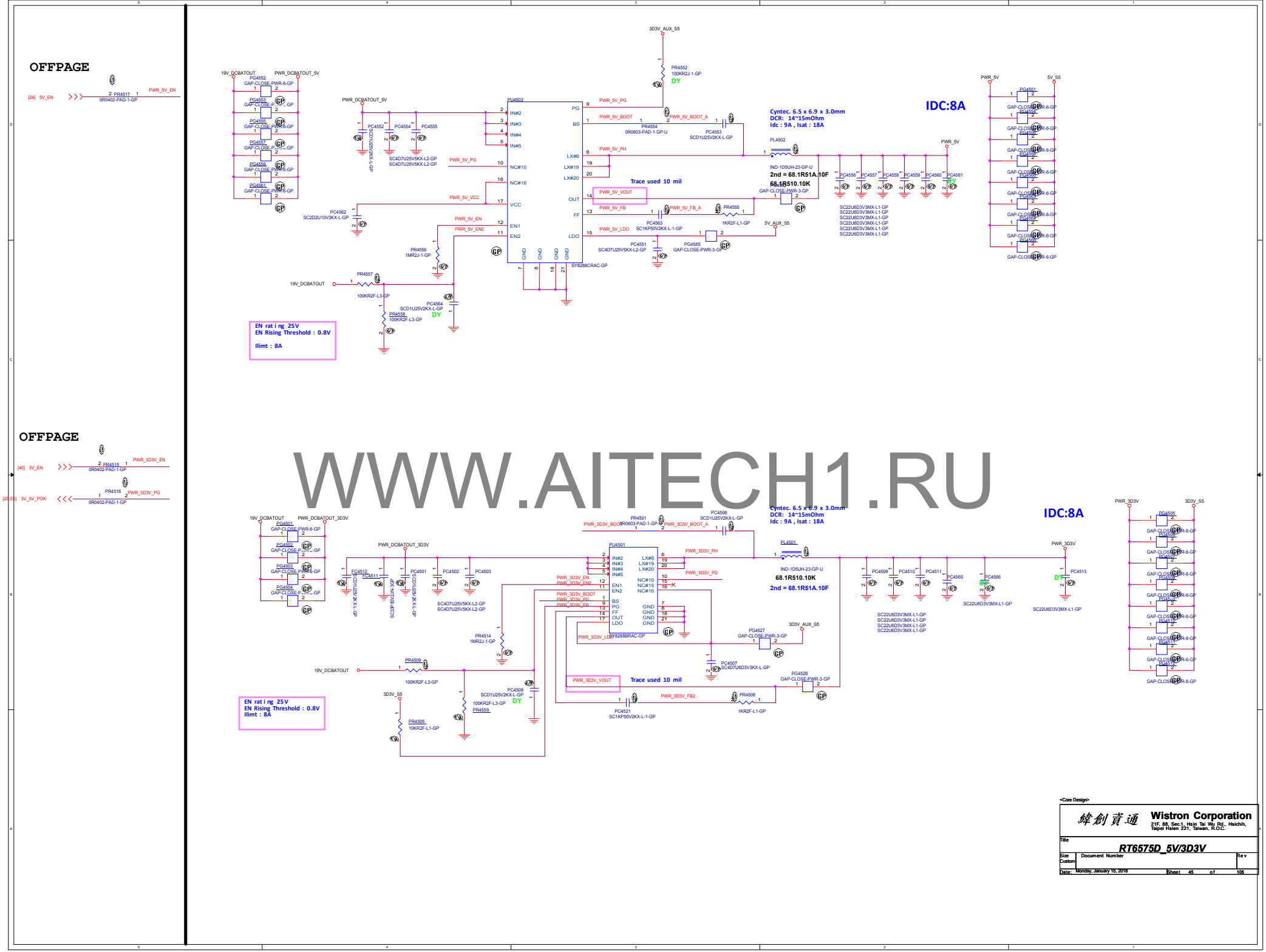
OFFPAGE
[24] 5V_EN
PR4517
PWR_5V_EN
0R0402-PAD-1-GP
OFFPAGE
[40] 3V_EN
[20,53] 3V_5V_POK
PR4515
PR4516
PWR_3D3V_EN
PWR_3D3V_PG
0R0402-PAD-1-GP
3D3V_AUX_S5
PR4552
100KR2J-1-GP
DY
19V_DCBATOUT
PWR_DCBATOUT_5V
PU4502
PWR_5V_PG
PWR_5V_BOOT
PWR_5V_BOOT_A
PWR_5V_PH
PWR_5V_VOUT
PWR_5V_FB
PWR_5V_FB_A
PWR_5V_LDO
PWR_5V_VCC
PWR_5V_EN
PWR_5V_EN2
SY8288CRAC-GP
Cyntec. 6.5 x 6.9 x 3.0mm
DCR: 14~15mOhm
Idc : 9A , Isat : 18A
IDC:8A
PL4502
IND-1D5UH-23-GP-U
2nd = 68.1R51A.10F
68.1R510.10K
Trace used 10 mil
PWR_5V
5V_S5
5V_AUX_S5
EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A
PWR_DCBATOUT_3D3V
PU4501
PWR_3D3V_BOOT
PWR_3D3V_BOOT_A
PWR_3D3V_PH
PWR_3D3V_PG
PWR_3D3V_EN
PWR_3D3V_EN2
PWR_3D3V_FB
PWR_3D3V_LDO
PWR_3D3V_VOUT
PWR_3D3V_FB2
PL4501
IND-1D5UH-23-GP-U
68.1R510.10K
2nd = 68.1R51A.10F
Trace used 10 mil
PWR_3D3V
3D3V_S5
EN rating 25V
EN Rising Threshold : 0.8V
Ilimt : 8A
WWW.AITECH1.RU
<Core Design>
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Title
RT6575D_5V/3D3V
Size
Custom
Document Number
Rev
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Main Func = CPU_CORE

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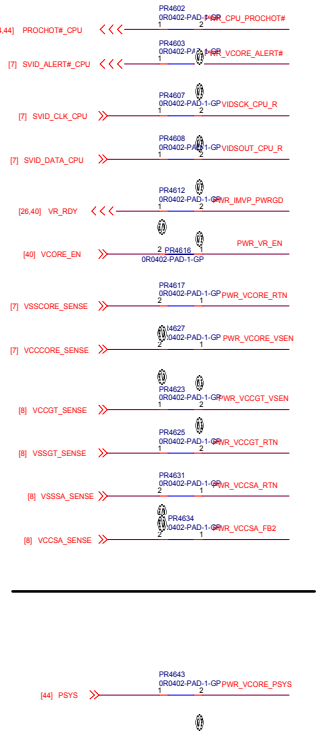

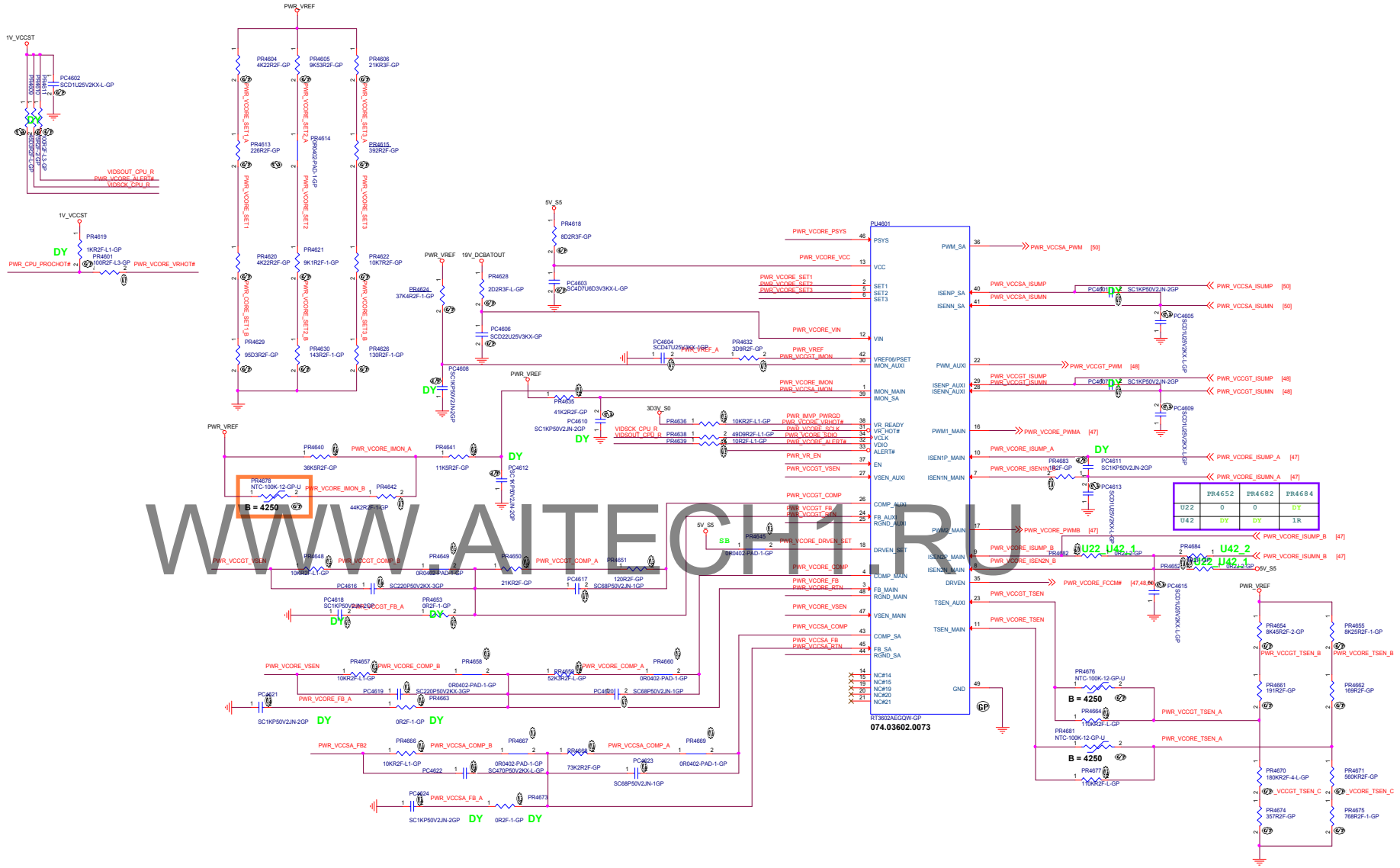

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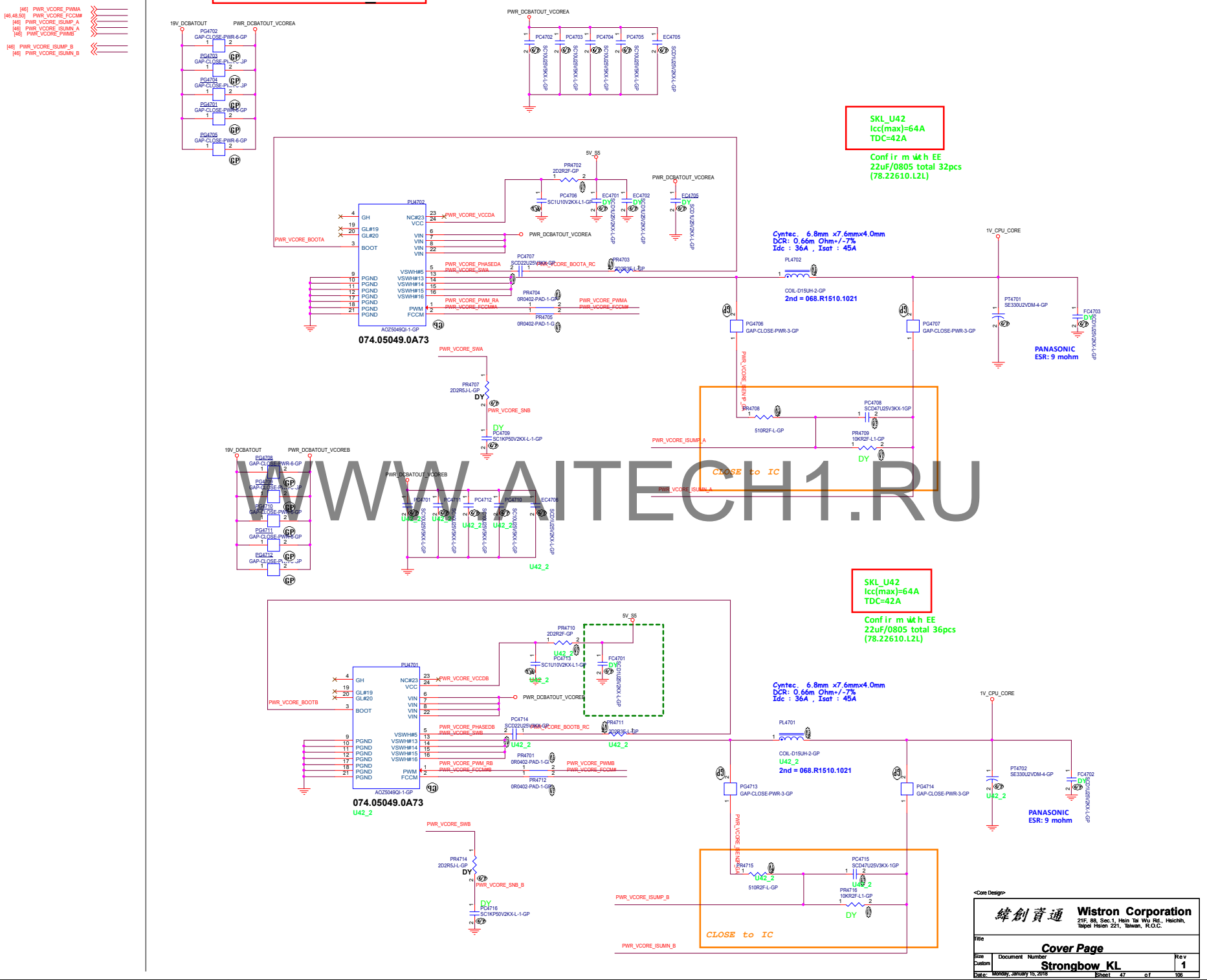

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Main Func = CPU_CORE

[46] PWR_VCCGT_PWM
[46,47,50] PWR_VCORE_FCCM#
[46] PWR_VCCGT_ISUMP
[46] PWR_VCCGT_ISUMN

19V_DCBATOUT
PWR_DCBATOUT_VCCGTA

PG4802 GAP-CLOSE-PWR-6-GP
PG4803 GAP-CLOSE-PWR-6-GP
PG4804 GAP-CLOSE-PWR-6-GP
PG4801 GAP-CLOSE-PWR-6-GP
PG4805 GAP-CLOSE-PWR-6-GP
PG4806 GAP-CLOSE-PWR-6-GP

PT4802 ST15U25VBM-GP
DY

PC4802 SC10U25V5KX-L-GP
PC4803 SC10U25V5KX-L-GP
PC4804 SC10U25V5KX-L-GP
PC4801 SC10U25V5KX-L-GP
EC4805 SCD1U25V2KX-L-GP

SKL_U42
Icc(max)=28A
TDC=12A

Confir m with EE
22uF/0805 total 26pcs
(78.22610.L2L)

PU4801
AOZ5049QI-1-GP
074.05049.0A73

PWR_VCCGT_BOOT
PWR_VCCGT_VCC_R
PWR_VCCGT_PHASE
PWR_VCCGT_SW
PWR_VCCGT_PWM_R
PWR_VCCGT_FCCM#_R
PWR_VCCGT_BOOT_RC
PWR_VCCGT_PWM
PWR_VCORE_FCCM#

PR4802 2D2R2F-GP
PC4805 SC1U10V2KX-L1-GP
EC4801 DY SCD1U25V2KX-L-GP
EC4802 DY SCD1U25V2KX-L-GP
PR4803 2D2R3F-L-GP
PC4806 SCD22U25V3KX-GP
PR4804 0R0402-PAD-1-GP
PR4805 0R0402-PAD-1-GP

5V_S5

PWR_DCBATOUT_VCCGTA
FC4805 DY SCD1U25V2KX-L-GP

Cyntec 6.8mm x7.6mmx4.0mm
DCR: 0.66m Ohm+/-7%
Idc : 36A , Isat : 45A

PL4801
COIL-D15UH-2-GP
2nd = 068.R1510.1021

1V_VCCGT

PG4807 GAP-CLOSE-PWR-3-GP
PG4808 GAP-CLOSE-PWR-3-GP
FC4801 SCD1U25V2KX-L-GP
EC4803 SCD1U25V2KX-L-GP
PT4801 SE330U2VDM-4-GP
DY

PWR_VCCGT_SW
PR4808 2D2R5J-L-GP
DY
_VCCGT_SNB
DY
PC4808 SC1KP50V2KX-L-1-GP

PWR_VCCGT_ISEN
PR4807 590R2F-GP
PC4807 SCD47U25V3KX-1GP
PR4809 487R2F-GP
PR4810 10KR2F-L1-GP
PWR_VCCGT_ISUMP
CLOSE to IC
PWR_VCCGT_ISUMN
PR4801 NTC-10K-29-GP-U
B = 3370

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Title: ***Cover Page***

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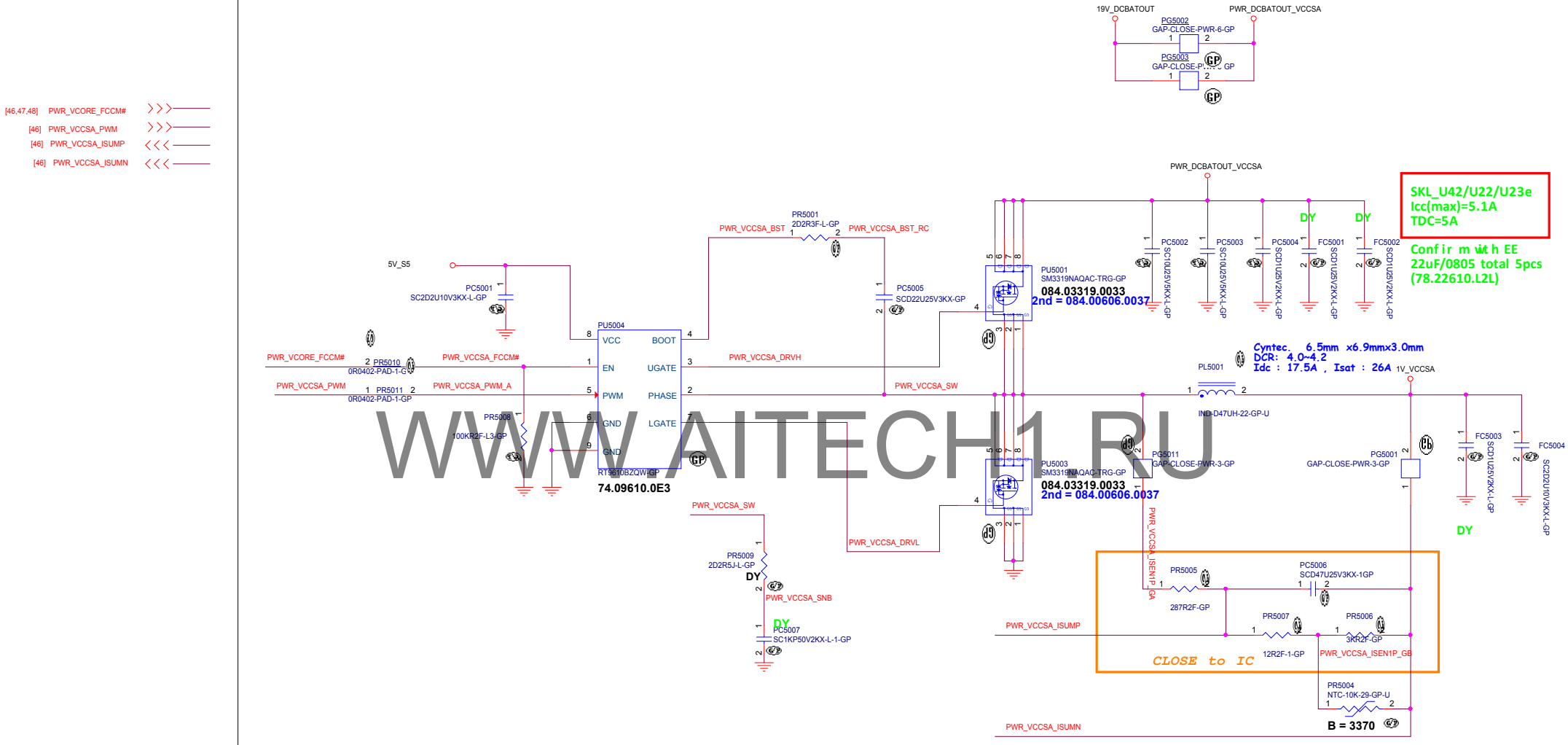

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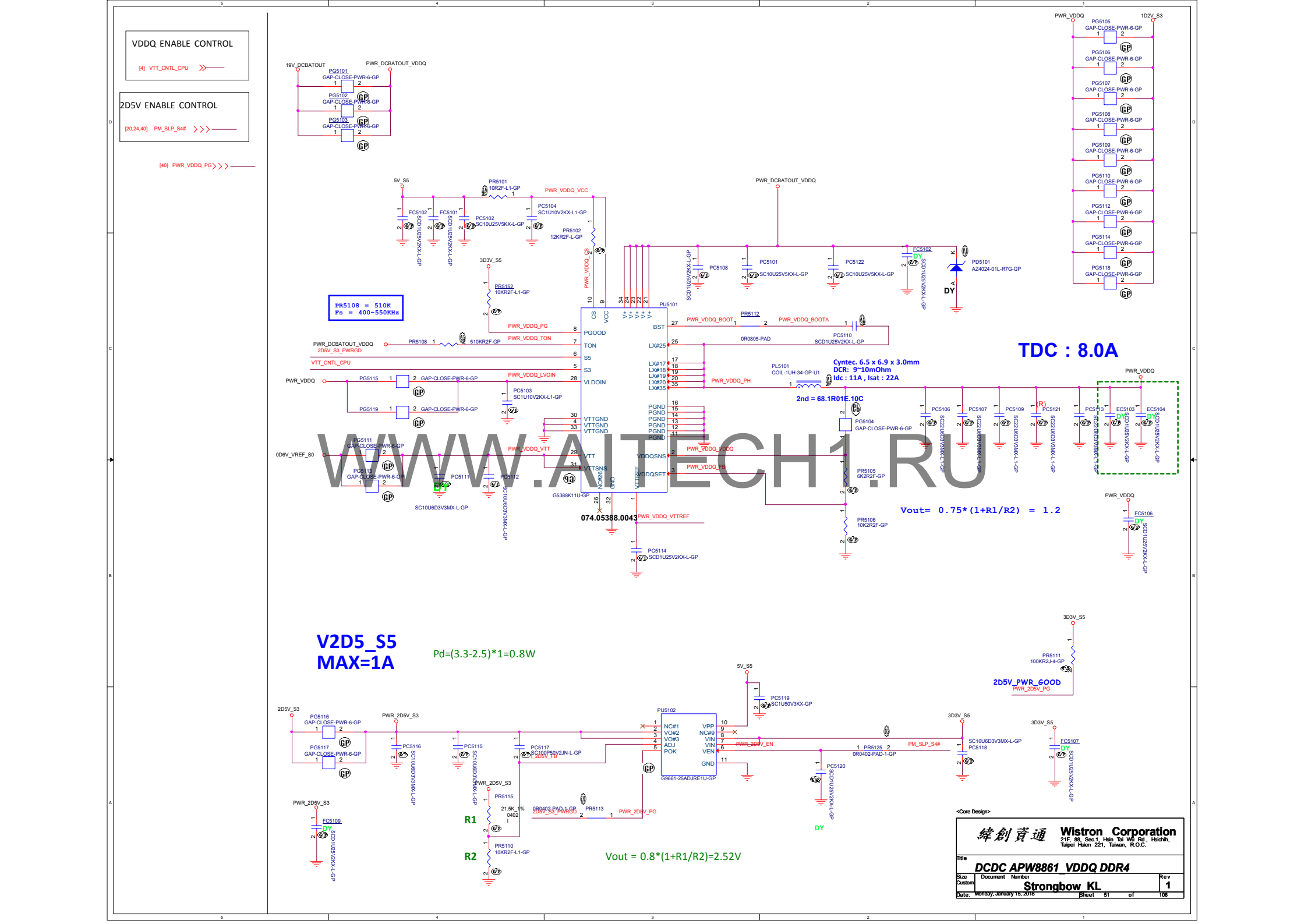
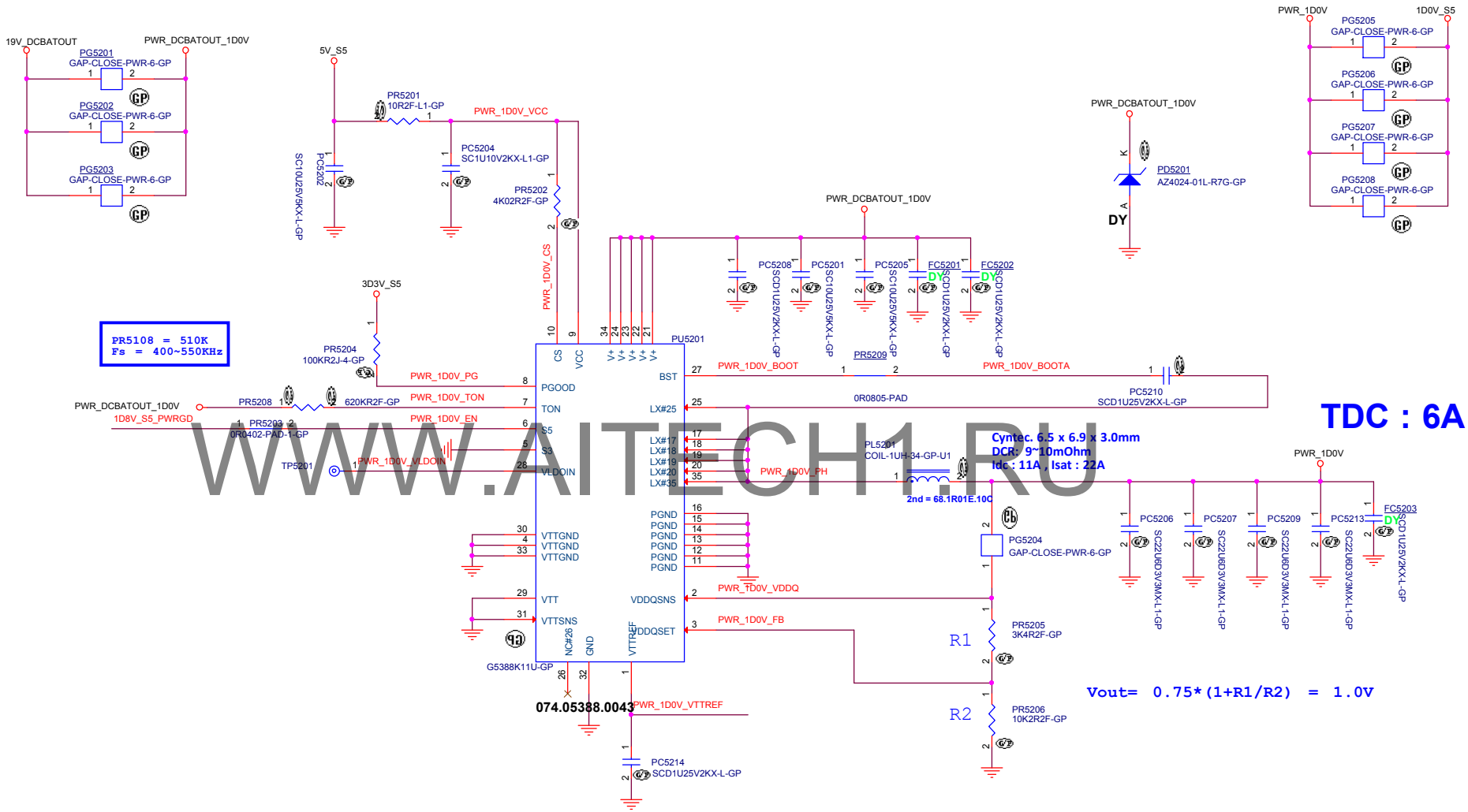


1D0V ENABLE CONTROL

[53] 1D8V_S5_PWRGD



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Title: RT8237_1D0V_S5

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1D8V_S5

1D8V_S5 POWER GOOD

[52] 1D8V_S5_PWRGD

[20,45] 3V_5V_POK

[0,24,40,58] PM_SLP_S3#

PD = (Vin Vout) x Iout
= (3.3 - 1.8) x 0.3A = 0.45W
PD de-rating(%) = 0.45W/1.33W = 33.8%

1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D

5V_S5
PR5302 2D2R2F-GP
PC5302 SC1U10V2KX-L1-GP
3D3V_S5
PG5301 GAP-CLOSE-PWR-6-GP
PG5302 GAP-CLOSE-PWR-3-GP
PC5303 SC10U6D3V3MX-L-GP
PC5304 SC10U6D3V3MX-L-GP
FC5301 SCD1U25V2KX-L-GP
3V_5V_POK
PR5301 0R0402-PAD-1-GP
PWR_1D8V_S5_EN
PC5307 SC1U10V2KX-L1-GP

PU5301
PWR_1D8V_S5_VDD
PWR_1D8V_S5_PVDD
PWR_1D8V_S5_EN
VPP NC#9 VIN VIN VEN GND
NC#1 VO#2 VO#3 ADJ POK
PWR_1D8V_S5_FB
1D8V_S5_PWRGD
G9661-25ADJRE1U-GP

R1 PR5303 12K7R2F-GP
PC5305 SC22P50V2JN-L-GP
PWR_1D8V_S5_FB
R2 PR5304 10KR2F-L1-GP

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

DY PC5306 SC10U6D3V3MX-L-GP
PC5301 SC10U6D3V3MX-L-GP
PWR_1D8V
PG5303 GAP-CLOSE-PWR-6-GP
PG5304 GAP-CLOSE-PWR-3-GP
1D8V_S5
PWR_1D8V
FC5310 SCD1U25V2KX-L-GP

3D3V_S5
PR5305 10KR2F-L1-GP
1D8V_S5_PWRGD

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

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Title: RT5797_1D8V
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Title

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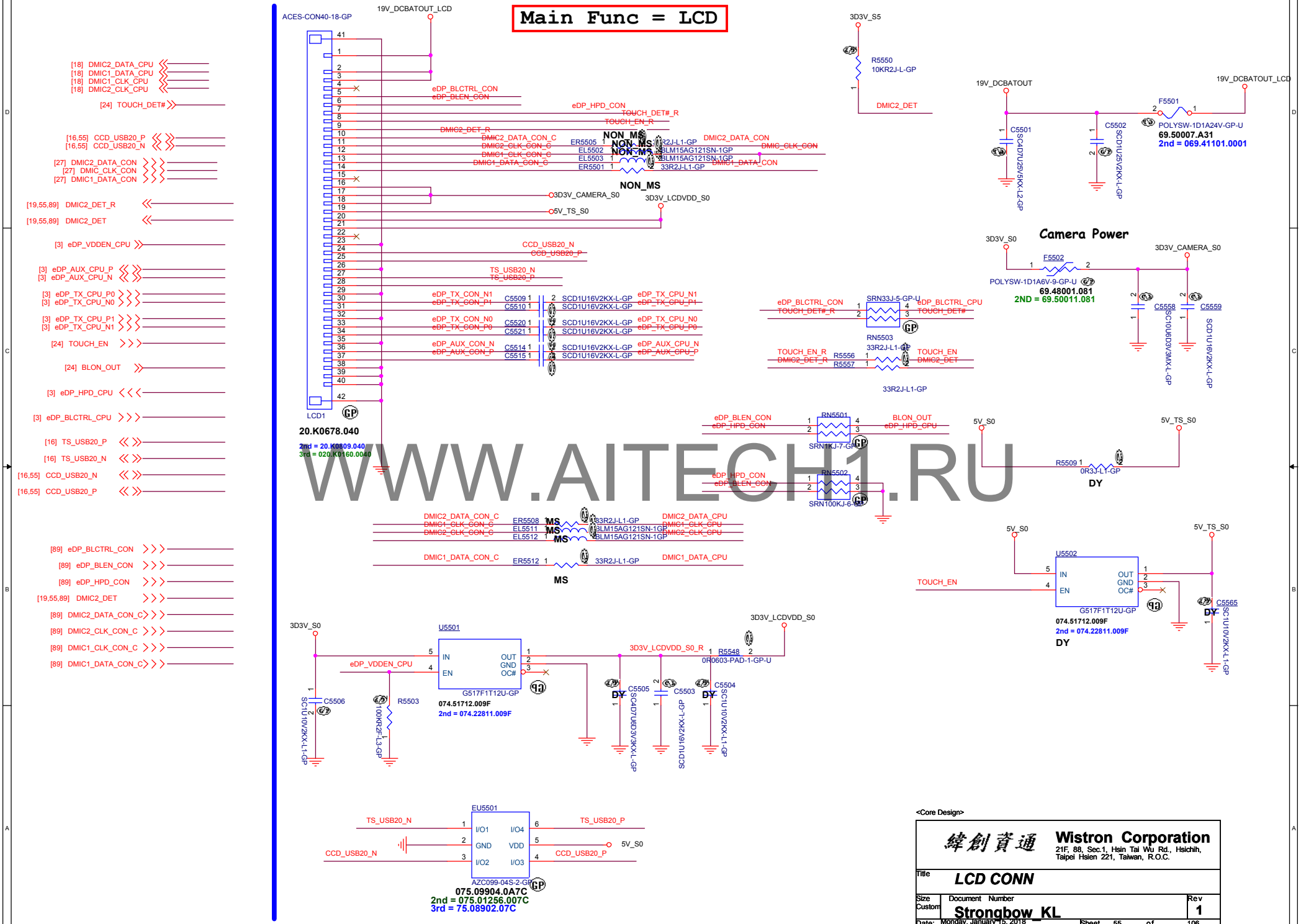
Main Func = LCD



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LCD CONN	
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Title

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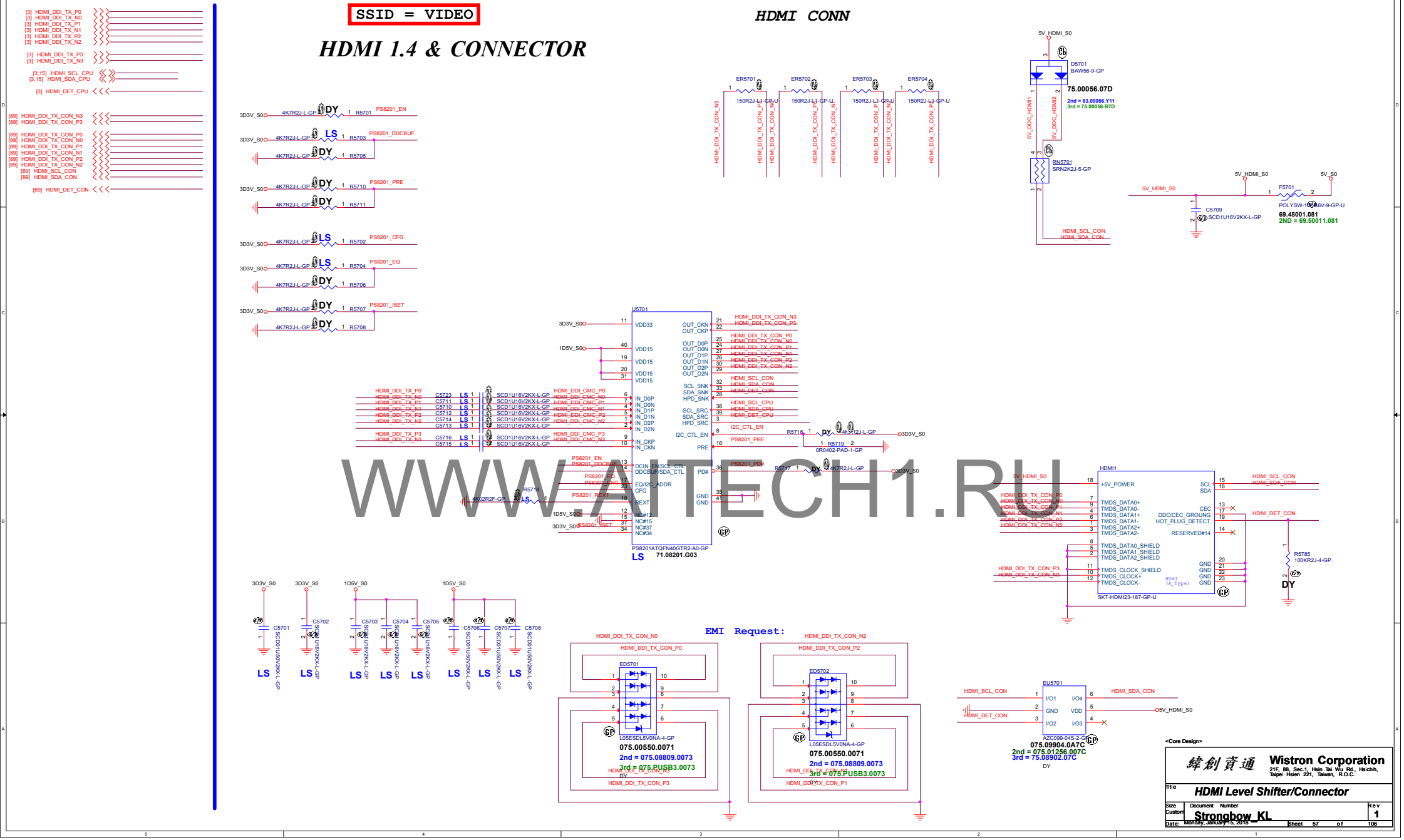
SSID = VIDEO

HDMI 1.4 & CONNECTOR

HDMI CONN



<Core Design>

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Title: HDMI Level Shifter/Connector

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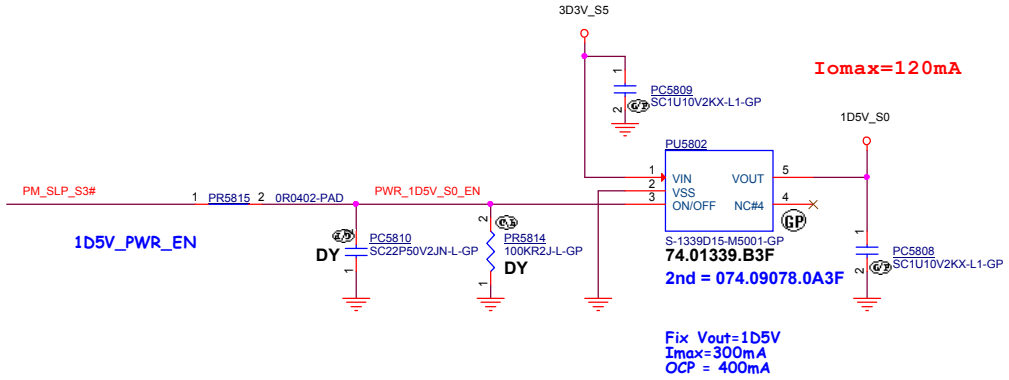
[20,24,40] PM_SLP_S3#



<Core Design>

緯創資通 Wistron Corporation
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Title: HDMI Power

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Title		
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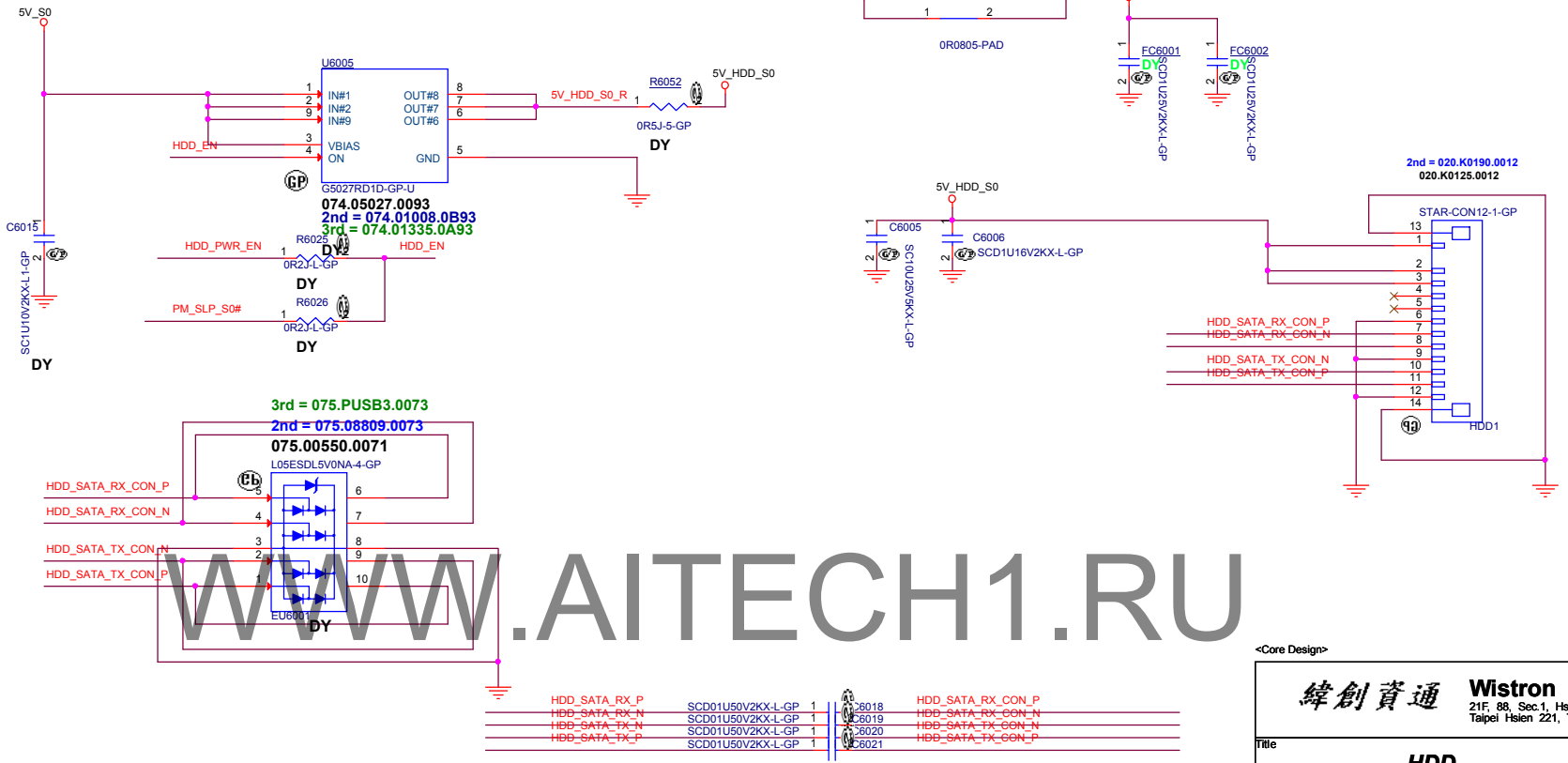
HDD_SATA_RX_P [16]
HDD_SATA_RX_N [16]
HDD_SATA_TX_N [16]
HDD_SATA_TX_P [16]
PM_SLP_S3# [20,24,40,58]
PM_SLP_S0# [20,24,40,91]
HDD_PWR_EN [6]

SSID = SATA

SATA HDD Connector



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Title: HDD

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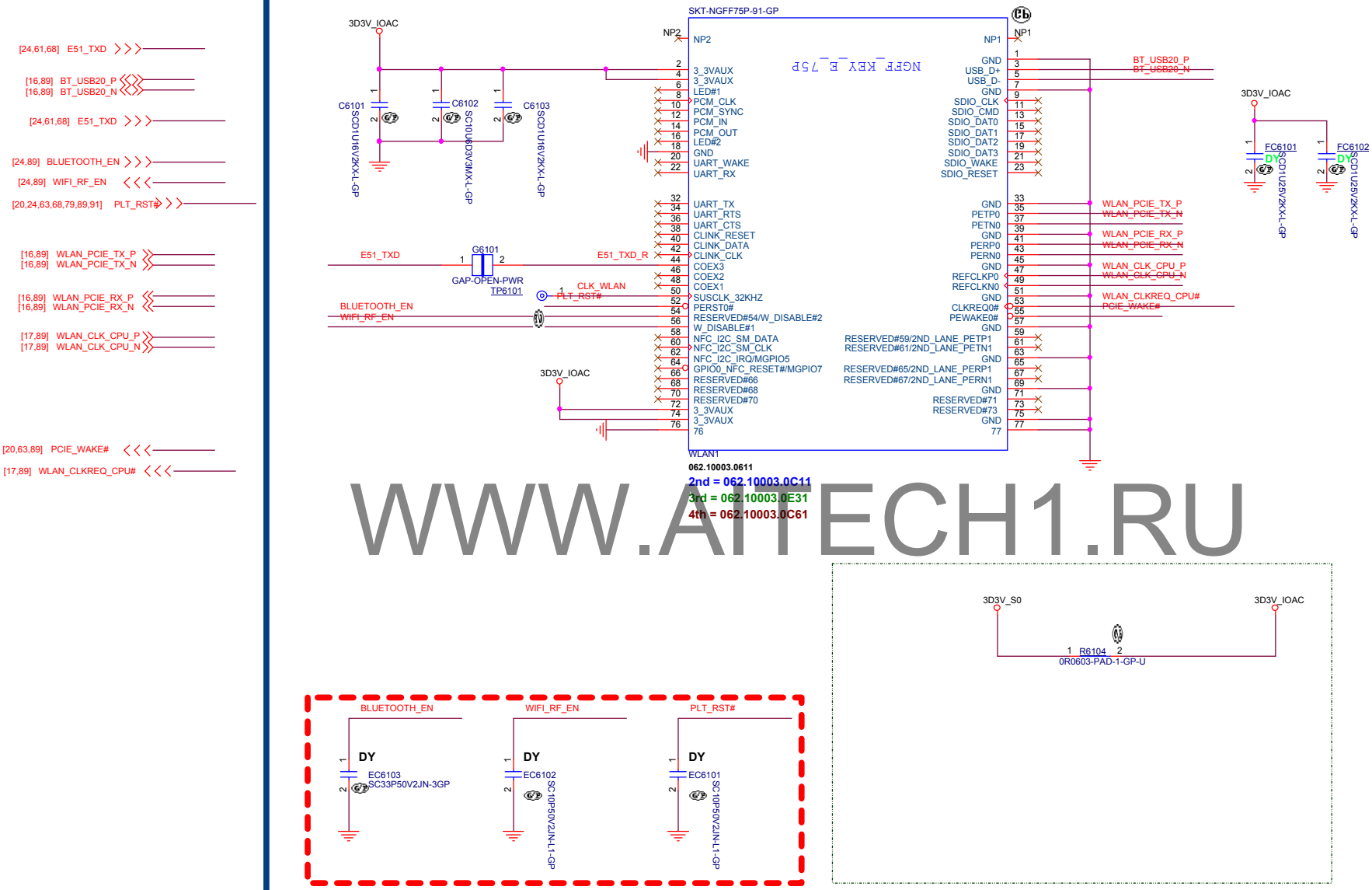
SSID = Wireless Mini Card Connector(802.11a/b/g/n)



[24,61,68] E51_TXD
[16,89] BT_USB20_P
[16,89] BT_USB20_N
[24,61,68] E51_TXD
[24,89] BLUETOOTH_EN
[24,89] WIFI_RF_EN
[20,24,63,68,79,89,91] PLT_RST#
[16,89] WLAN_PCIE_TX_P
[16,89] WLAN_PCIE_TX_N
[16,89] WLAN_PCIE_RX_P
[16,89] WLAN_PCIE_RX_N
[17,89] WLAN_CLK_CPU_P
[17,89] WLAN_CLK_CPU_N
[20,63,89] PCIE_WAKE#
[17,89] WLAN_CLKREQ_CPU#

<Core Design>

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Title: Mini Card-WLAN

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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<Core Design>

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Title: ***(Reserved)WWAN***

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SSID = mSATA

Mini Card Connector(mSATA)

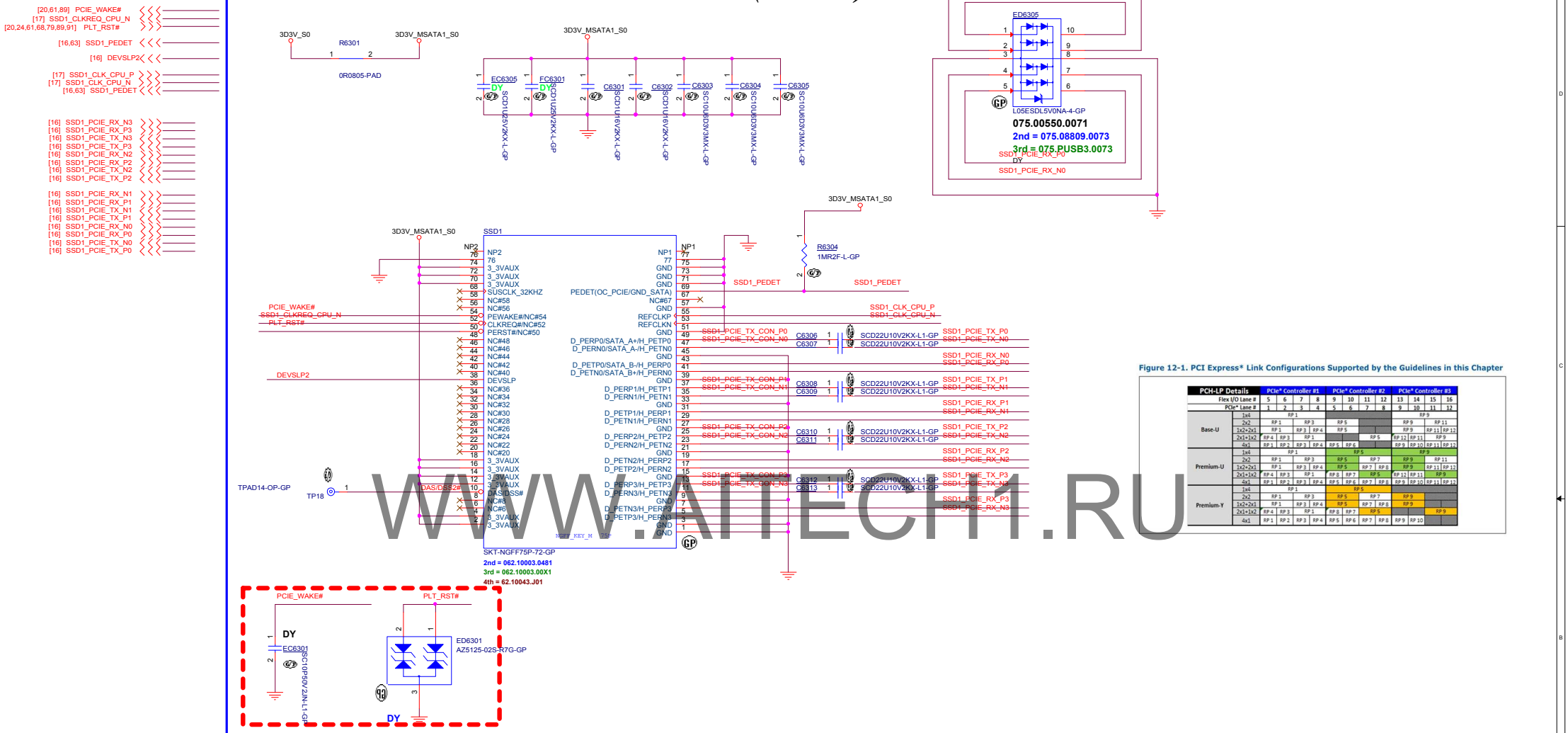

Figure 12-1. PCI Express* Link Configurations Supported by the Guidelines in this Chapter

PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP 1								RP 9			
	2x2	RP 1		RP 3		RP 5				RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5				RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1				RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6			RP 9	RP 10	RP 11	RP 12
Premium-U	1x4	RP 1				RP 5				RP 9			
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9		RP 11	
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9		RP 11	RP 12
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5		RP 12	RP 11	RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10	RP 11	RP 12
Premium-Y	1x4	RP 1				RP 5							
	2x2	RP 1		RP 3		RP 5		RP 7		RP 9			
	1x2+2x1	RP 1		RP 3	RP 4	RP 5		RP 7	RP 8	RP 9			
	2x1+1x2	RP 4	RP 3	RP 1		RP 8	RP 7	RP 5				RP 9	
	4x1	RP 1	RP 2	RP 3	RP 4	RP 5	RP 6	RP 7	RP 8	RP 9	RP 10		

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

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Title: SSD-NGFF-1

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Title: ***LED Bard/Power Button***

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SSID = KBC

[24,89] KSI[0..7]
[24,89] KSO[0..17]
[24] EC_TPCLK
[24] EC_TPDATA
[24,89] FUN_OFF#
[89] EC_TP_CLK_C
[89] EC_TP_DATA_C
[89] I2C1_DATA_TP
[89] I2C1_CLK_TP
[24] PTP_PWR_EN
[22] TP_IN#
[24,89] EC_TP_IN#
[24,89] EC_TP_IN_R#
[6] PM_TP_CLK
[6] PM_TP_DATA
[24] KB_BL_PWM
[24] KB_BL_DET
[89] KB_BL_DET_R
[89] KB_LED_PWM_R
[24,64,89] KBC_PWRBTN#

3D3V_TP_S3
3D3V_S0
RN6505 SRN2K2J-5-GP
PM_TP_CLK
PM_TP_DATA
I2C1_CLK_TP
I2C1_DATA_TP
Q6503
75.27002.E7C
2nd = 075.67002.007C
3rd = 075.27002.0E7C
EC6504 DY SCD1U16V2KX-L-GP
EC6505 DY SCD1U16V2KX-L-GP

3D3V_TP_S3
R6506 100KR2F-L3-GP
3D3V_S0
Q6502
TP_IN#
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31
EC_TP_IN#
R6518 33R2J-L-GP
EC_TP_IN_R#
EC6507 DY SCD1U16V2KX-L-GP

3D3V_S5
U6502
PTP_PWR_EN
IN EN OUT GND OC#
G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
C6509 SC4D7U6D3V3KX-L-GP
3D3V_TP_S3_R
R6558 0R0603-PAD-1-GP-U
3D3V_TP_S3
C6504 SC4D7U6D3V3KX-L-GP

TOUCH PAD
3D3V_TP_S3
RN6503 SRN4K7J-8-GP
EC_TPCLK
EC_TPDATA
RN6502 SRN33J-5-GP-U
FUN_OFF#
EC6502 SC22P50V2JN-L-GP DY
EC_TP_CLK_C
EC_TP_DATA_C
I2C1_DATA_TP
I2C1_CLK_TP
EC_TP_IN_R#
EC6501 SC22P50V2JN-3GP DY
EC6503 SC22P50V2JN-3GP DY
TP1
STARCONN8-2-GP
020.K0182.0008
2nd = 020.K0243.0008

Internal KeyBoard Connector

KB1
ACES-CON28-10-GP
020.K0173.0028
2nd = 020.K0266.0028
KBC_PWRBTN#

PTWO-CON6-16-GP
KBBL1
KB_BL
KB_BL_DET_R
KB_LED_PWM_R
R6504 100KR2F-L3-GP
KB_BL_DET
R6502 200KR2F-L-3-GP
5V_S0
C6501 DY SCD1U16V2KX-L-GP
Q6501
2N7002K-2-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31
KB_BL_PWM

Circuit Diagram

<Core Design>

緯創資通 Wistron Corporation
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Title: Key Board/Touch Pad
Size: Custom
Document Number: Strongbow_KL
Rev: 1
Date: Monday, January 15, 2018
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[24,66,89] STDBY_LED
[24,66,89] POWER_LED
[24,66,89] CHARGE_LED
[24,66,89] DC_BATFULL
[24,66,89] LID_CLOSE#
[43,66,89] BI_RST
[16,89] USB4_USB20_N
[16,89] USB4_USB20_P
[16,89] CR_USB20_N
[16,89] CR_USB20_P
[24,35] USB_PWR_EN
[16,89] FP_USB20_N
[16,89] FP_USB20_P
3D3V_CR_S0
3D3V_AUX_S5
[24,66,89] STDBY_LED
[24,66,89] POWER_LED
[24,66,89] DC_BATFULL
[24,66,89] CHARGE_LED
5V_AUX_S5
5V_USB20
5V_S5
[24,66,89] LID_CLOSE#

SSID = User.Interface

Close connector

High Active 2A

U6601
G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
C6608 SC1U10V2KX-L1-GP
C6609 SCD1U16V2KX-L-GP

EU6602
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.08902.07C

EU6603
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.08902.07C

R6648 0R0805-PAD
R6649 0R0805-PAD

ACES-CON30-20-GP-U
20.K0848.030
2nd = 020.K0190.0030
3rd = 20.K0809.030

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Title: Reserved
Size: Custom
Document Number: Strongbow_KL
Rev: 1
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<Core Design>

緯創資通 Wistron Corporation
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Title: ***Reserved***

Size	Document Number	Rev
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Date: Thursday, January 11, 2018 Sheet 67 of 106

[19,24,91] INT_SERIRQ
[19] LPC_CLK_DBG

[20,24,61,63,79,89,91] PLT_RST#
[19,24,91] LPC_FRAME#_CPU

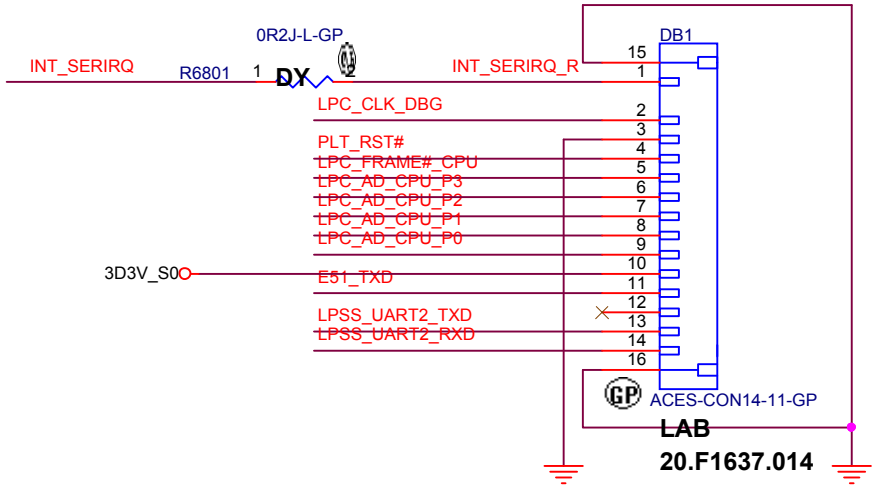
[19,24,91] LPC_AD_CPU_P3
[19,24,91] LPC_AD_CPU_P2

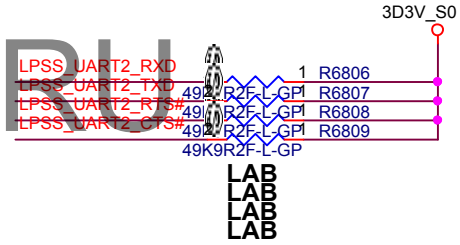
[19,24,91] LPC_AD_CPU_P1
[19,24,91] LPC_AD_CPU_P0

[24,61] E51_TXD

[6,68] LPSS_UART2_TXD
[6,68] LPSS_UART2_RXD

[6,68] LPSS_UART2_RXD
[6,68] LPSS_UART2_TXD
[6] LPSS_UART2_RTS#
[6] LPSS_UART2_CTS#





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Title: ***Dubug connector***

Size	Document Number	Rev
A4	Strongbow_KL	1

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<Core Design>

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Title

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SSID = User.Interface

G Sensor

<Core Design>

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Title: G SENSOR

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Thunderbolt (4/5)***

Size	Document Number	Rev
A4	Strongbow_KL	1

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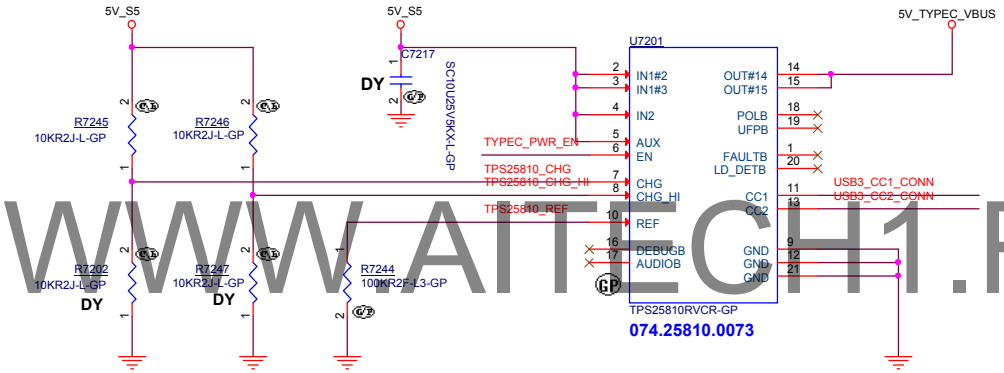
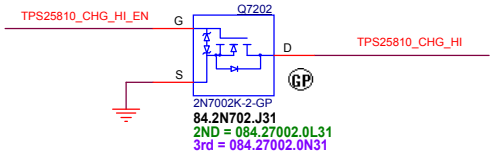
[24] TPS25810_CHG_HI_EN
[24] TYPEC_PWR_EN
[73,89] USB3_CC1_CONN
[73,89] USB3_CC2_CONN





CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

<Core Design>
Type_C CC
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Title
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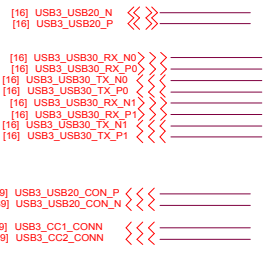
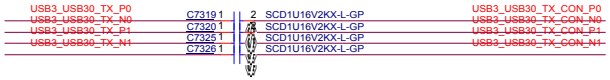
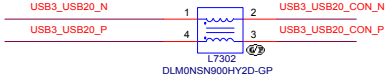
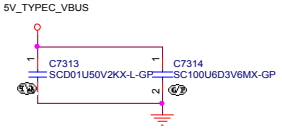
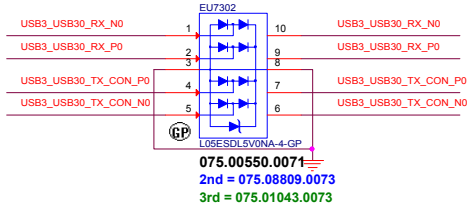
USB HOST

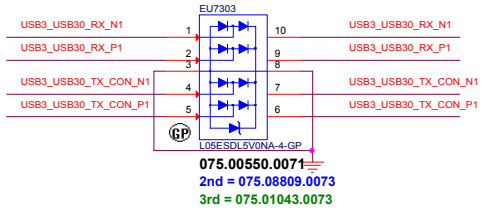


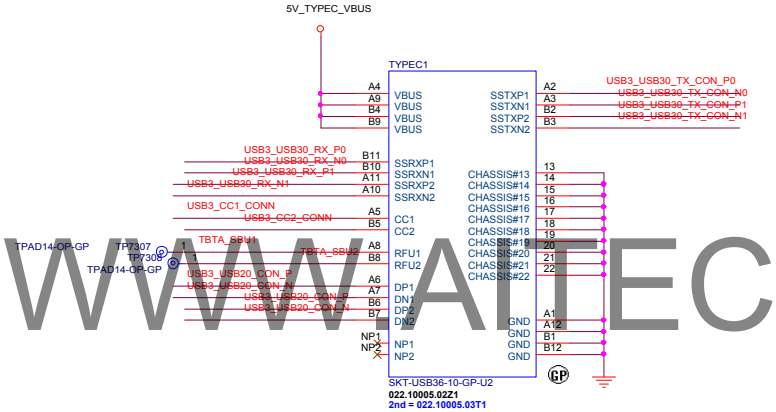


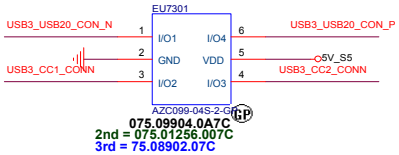












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Title	TYPE-C	
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緯創資通

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Title

GPU (DIGITALOUT)

Size	Document Number	Rev
A4	**Strongbow_KL**	**1**

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<Core Design>

緯創資通 Wistron Corporation
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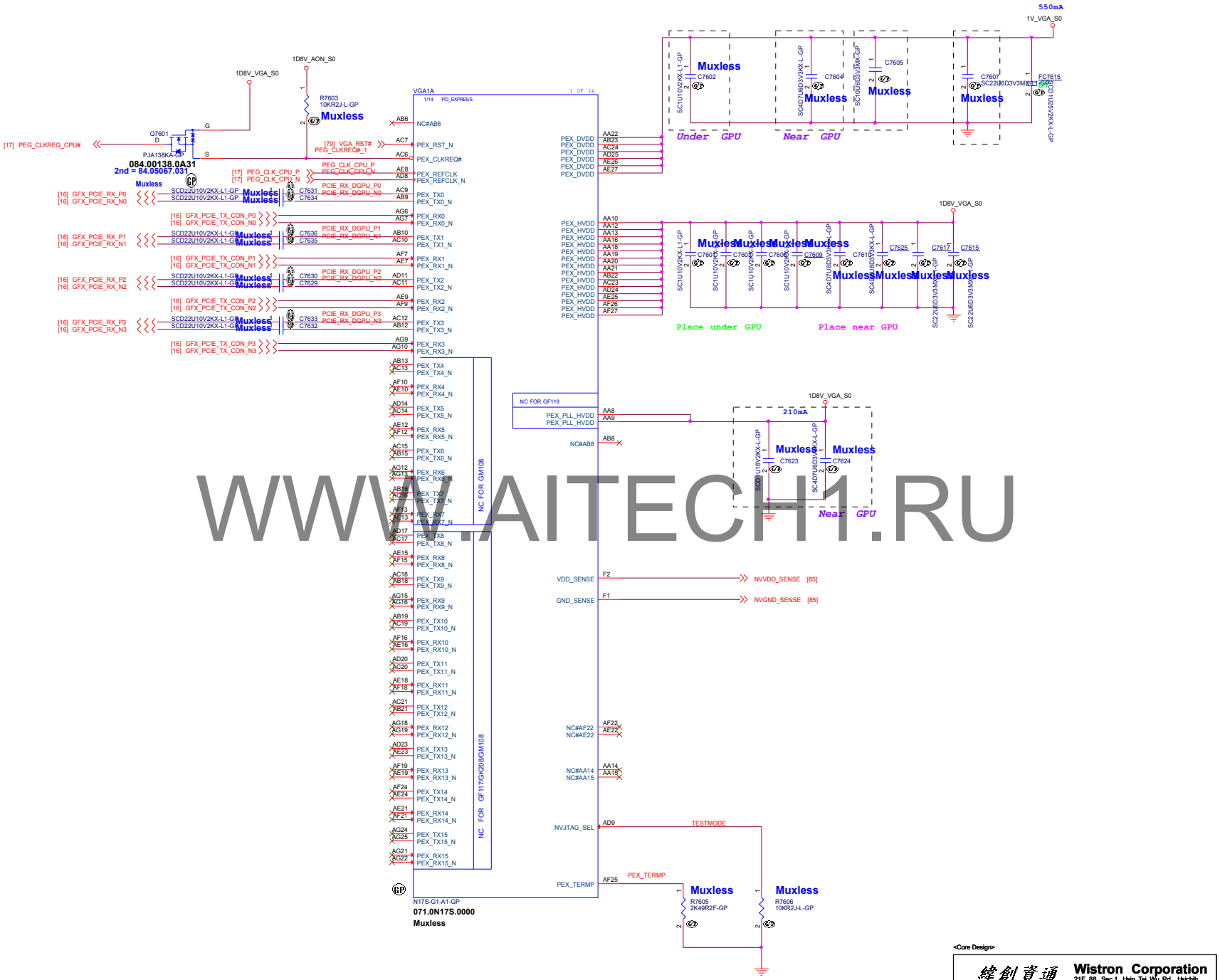
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU (VRAM I/F)

Size	Document Number	Rev
A4	Strongbow_KL	1

Date: Thursday, January 11, 2018 Sheet 75 of 106



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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5) PEG

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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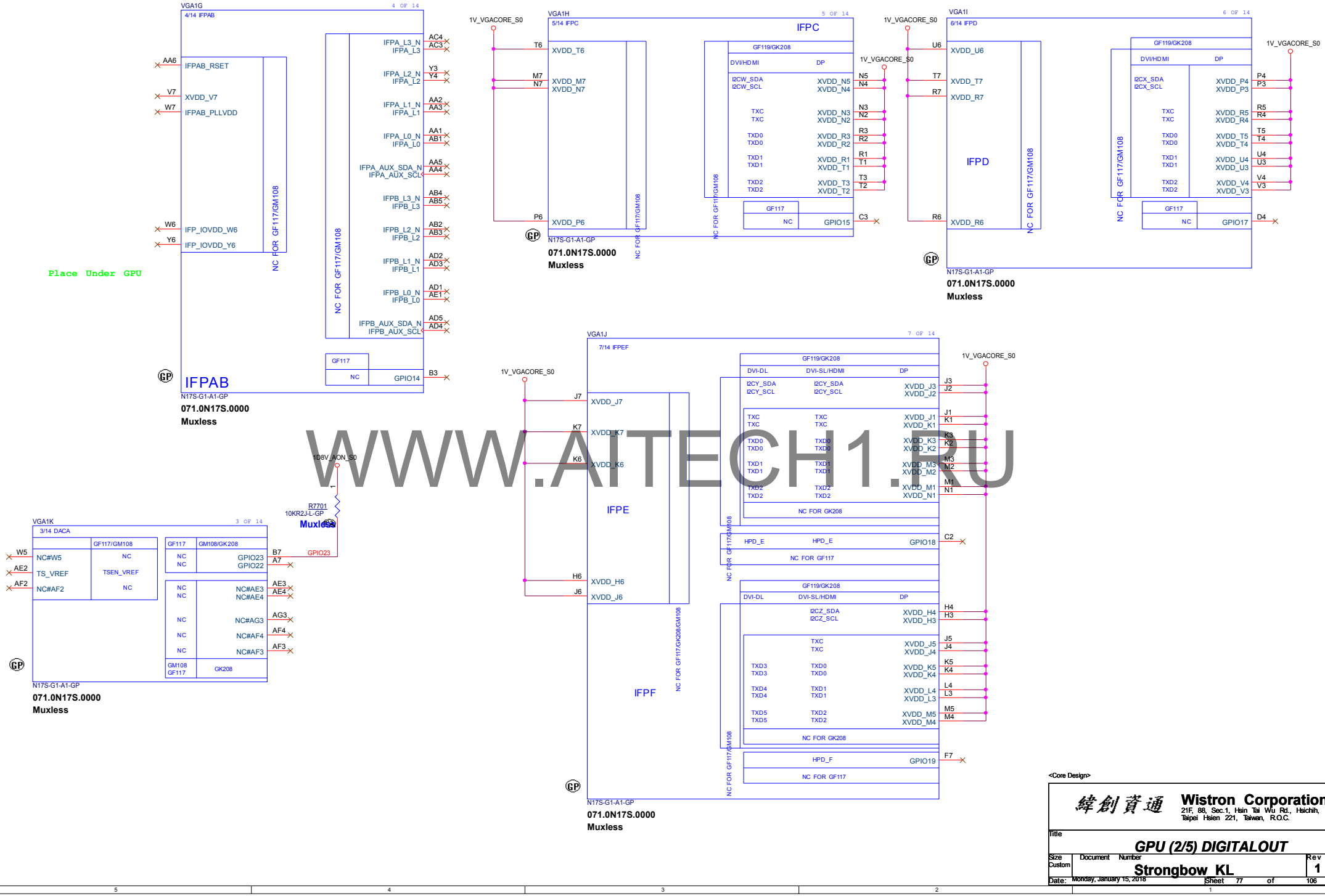

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Title: GPU (2/5) DIGITALOUT

Size: Custom | Document Number: Strongbow_KL | Rev: 1

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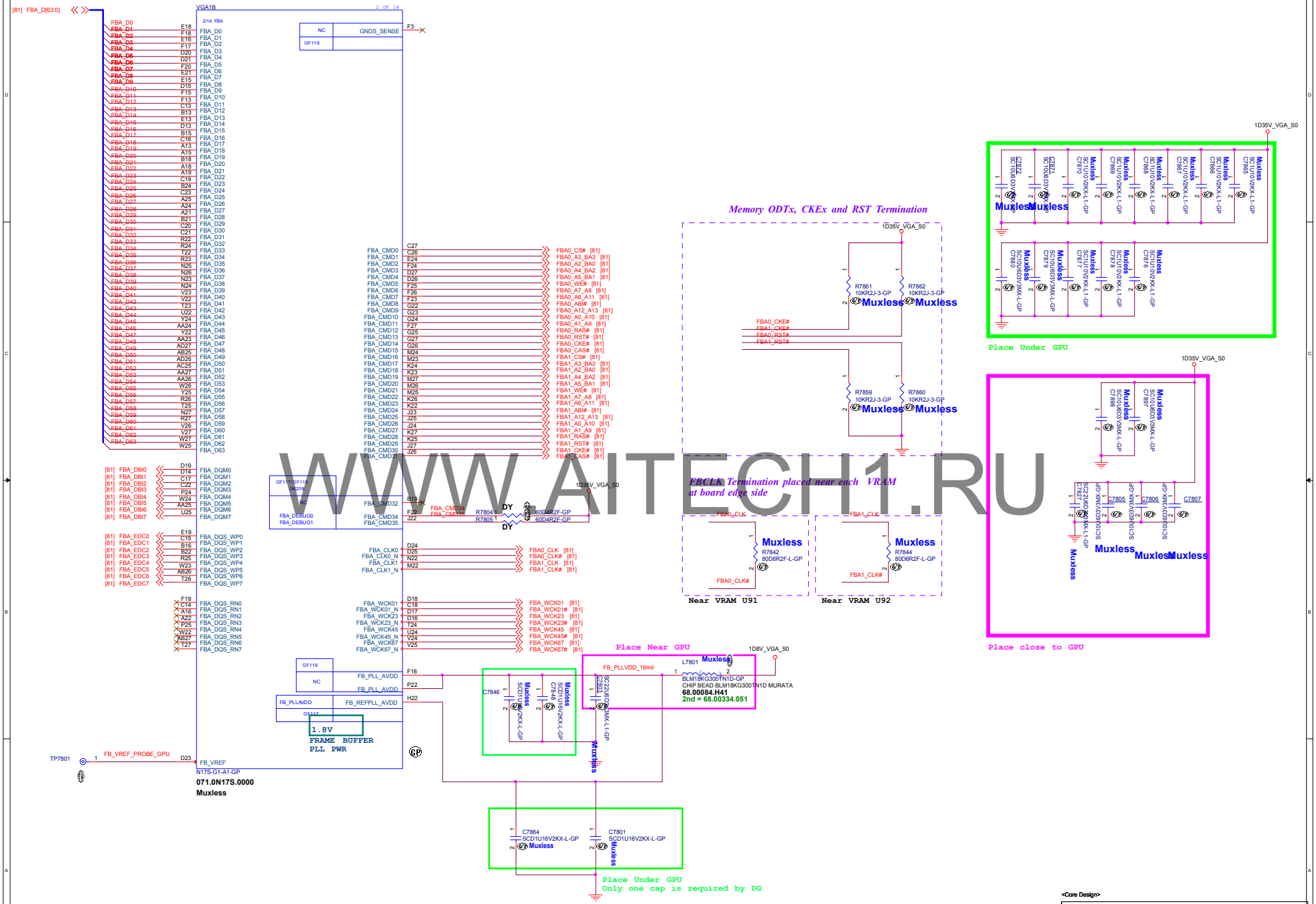
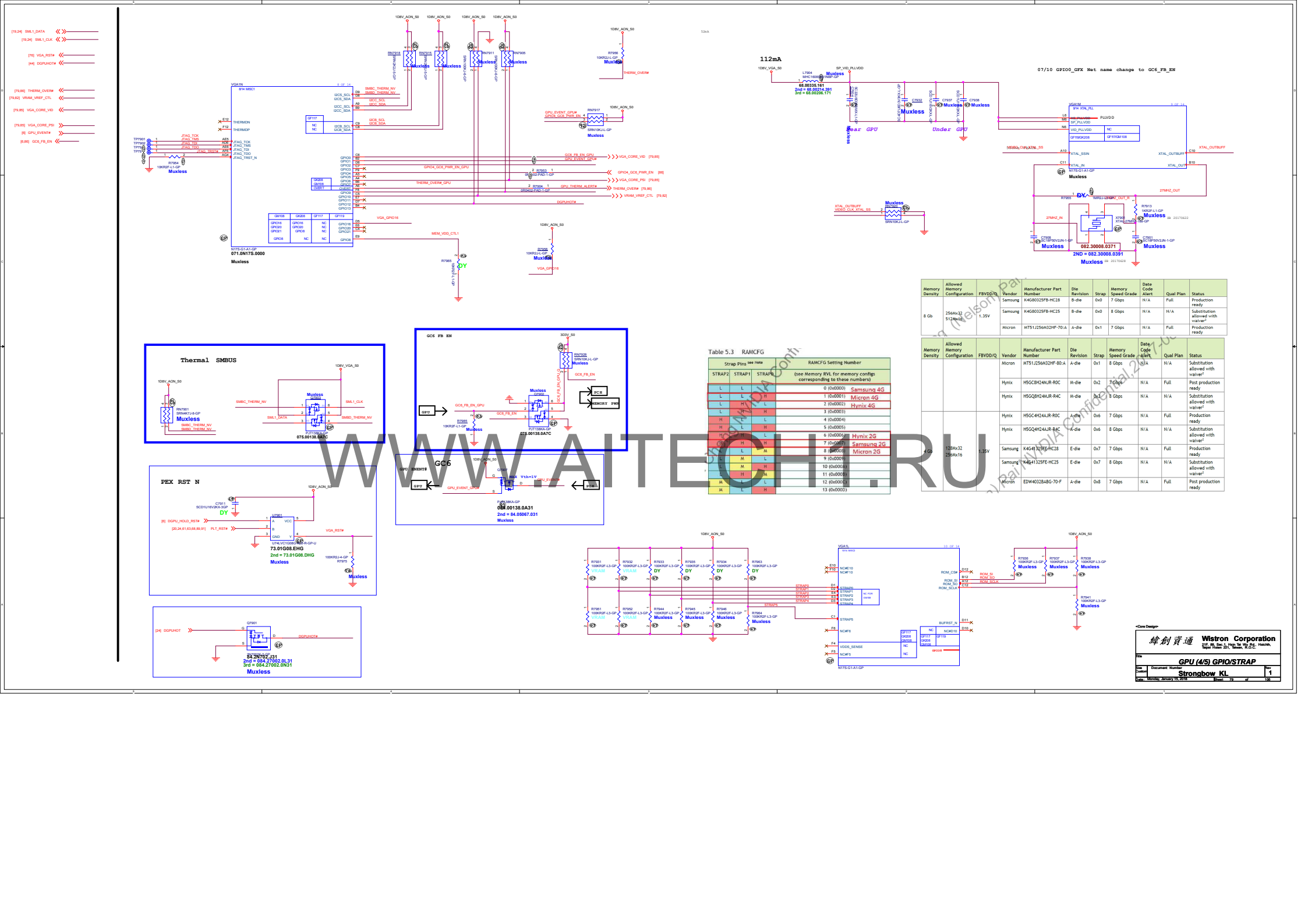
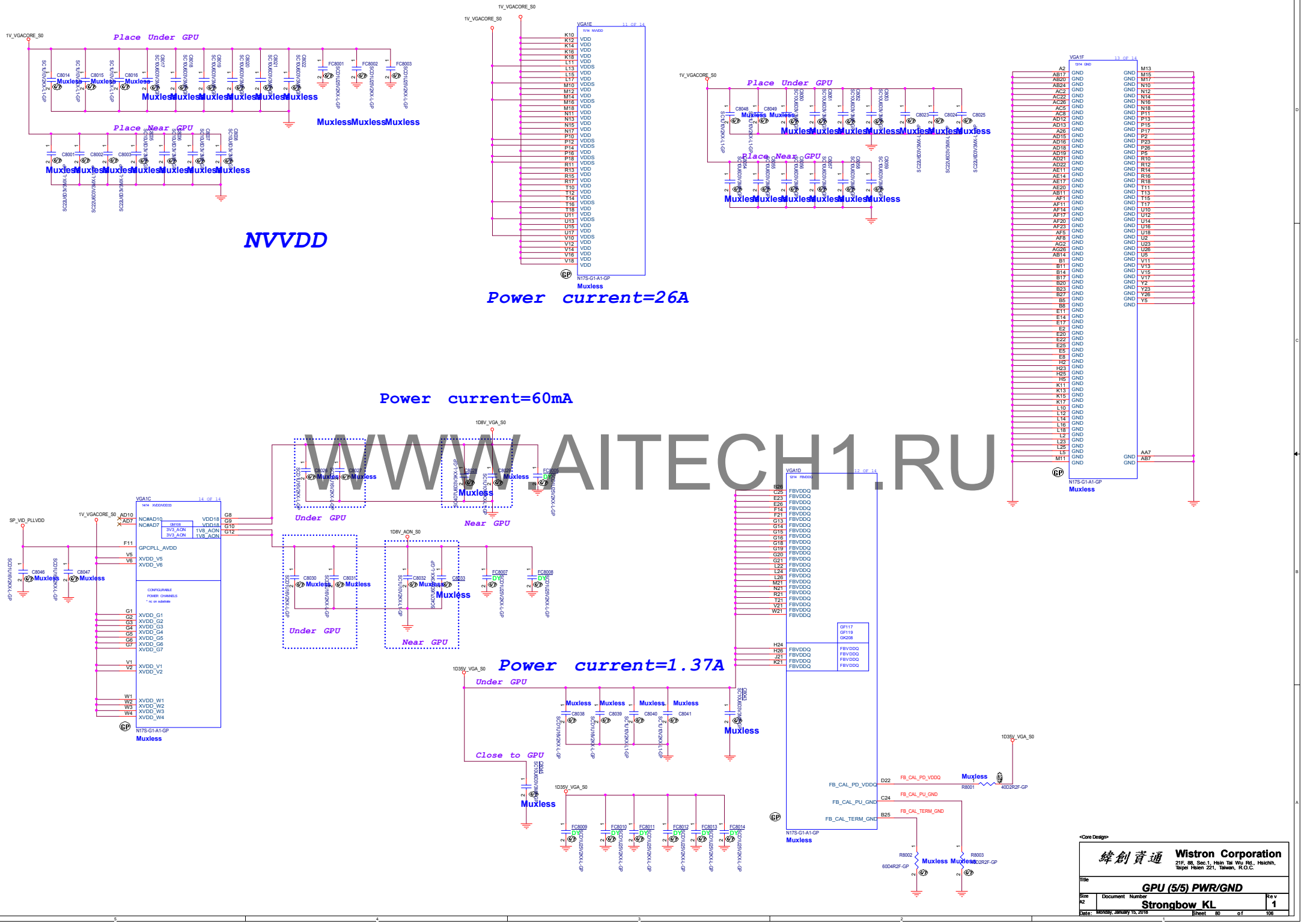




Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready

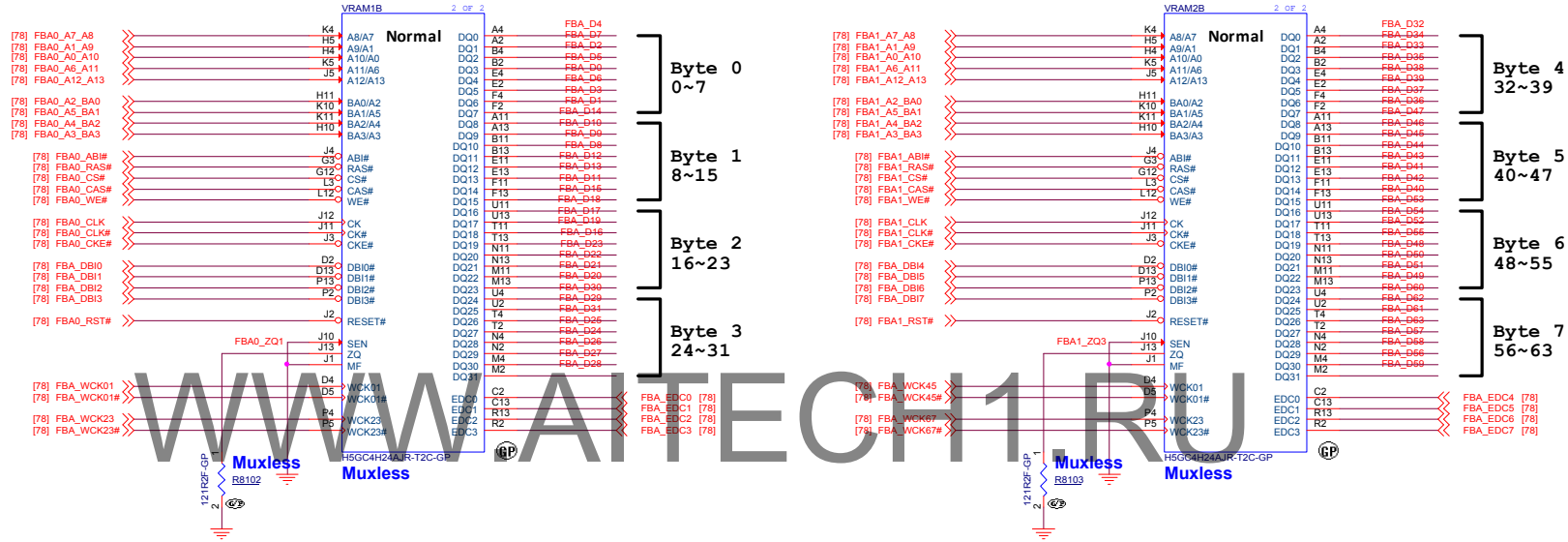
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
4 GB	128Mx32 256Mx16	1.35V	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production ready
			Hynix	H5GQ4H24AJR-R4C	A-die	0x6	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production ready
			Samsung	K4G41325FE-HC25	E-die	0x7	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production ready



[78] FBA_D[63:0]

TABLE
GDDR5 VIDEO MEMORY

	072.05424.0A0U	072.44132.000U	072.04032.000N
	HYNIX 4GBITS (128Mx32)	SAMSUNG 4GBITS (128Mx32)	Micron 4GBITS (128Mx32)
VRAM1 VRAM2	H5GC4H24AJR-T2C	K4G41325FC-HC03	EDW4032BABG-60-F-D



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Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM CHANNEL-A

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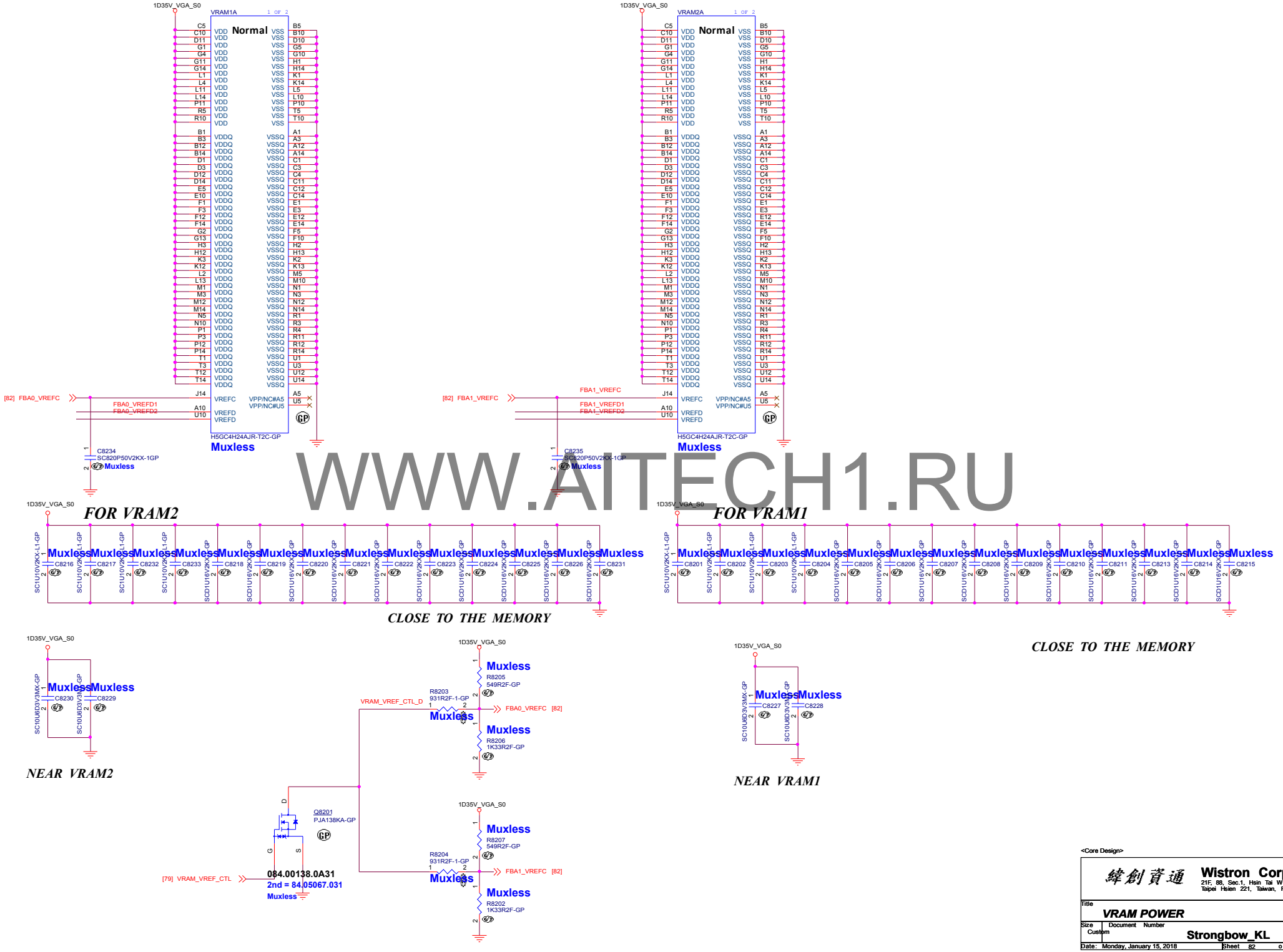

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Title: VRAM POWER

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Title: ***VRAM CHANNEL-B***

Size	Document Number	Rev
A2	Strongbow_KL	1

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<Core Design>

緯創資通 **Wistron Corporation**
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Title
MEMORY TERMINATION

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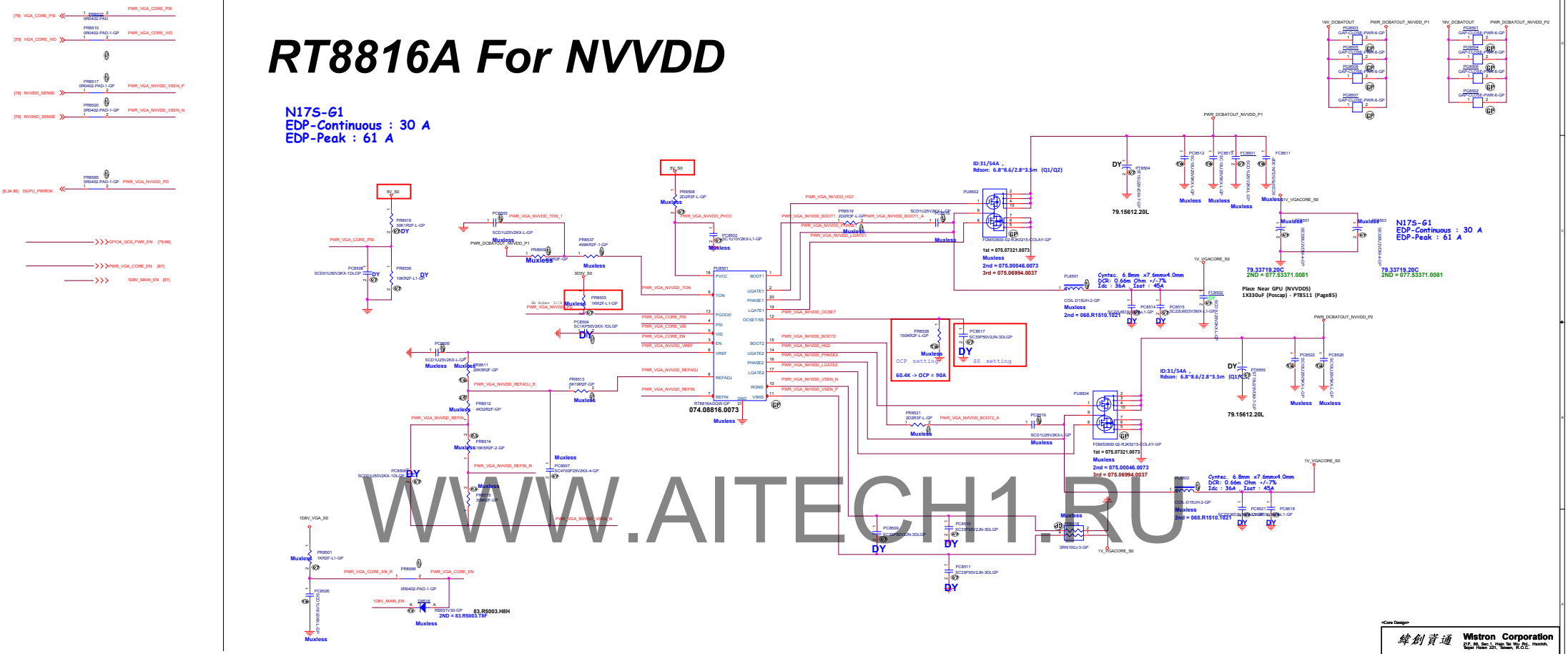
OFFPAGE

RT8816A For NVVDD

N17S-G1
EDP-Continuous : 30 A
EDP-Peak : 61 A



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Title: RT8816A/RT8813D VGA CORE

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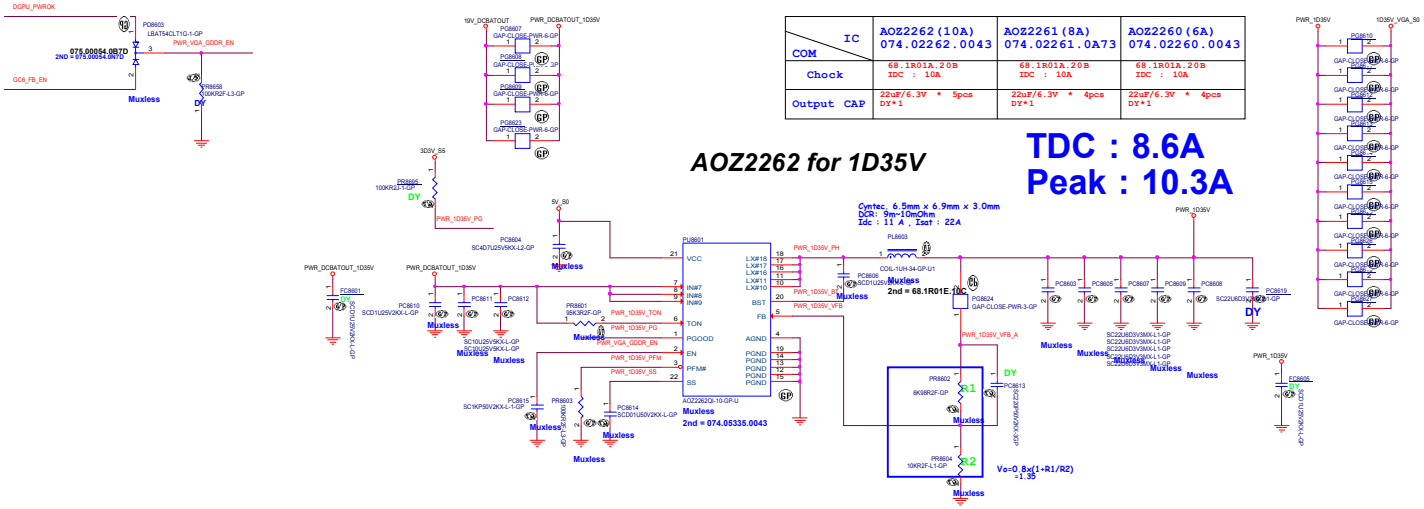
SSID = PWR.Plane.Regulator_1p0v

SSID = PWR.Plane.Regulator_1p35v

IC / COM	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 for 1D35V

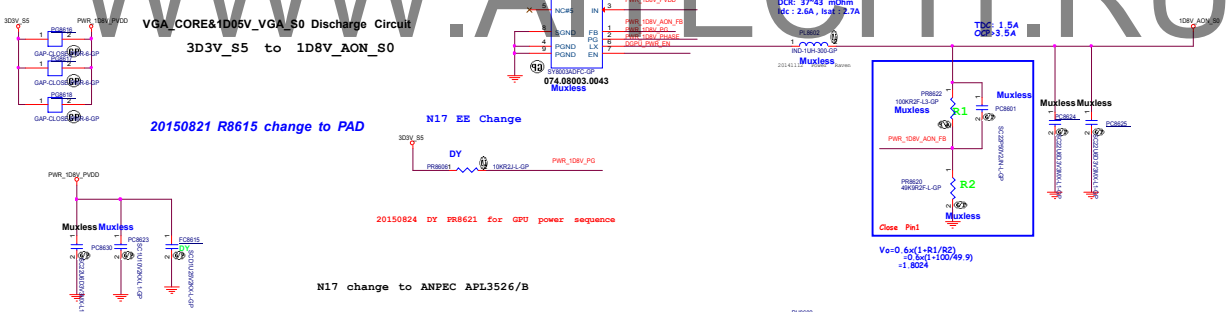
TDC : 8.6A
Peak : 10.3A



SYW232 for 1D8V_AON

VGA_CORE&1D05V_VGA_S0 Discharge Circuit

3D3V_S5 to 1D8V_AON_S0



20150821 R8615 change to PAD

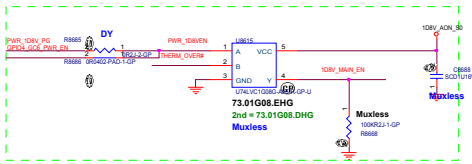
N17 EE Change

20150824 DY PR8621 for GPU power sequence

N17 change to ANPEC APL3526/B

SYW232 for 1D05V
Enable=1.5V
Disable=0.4V

SYW232 for 1D8V_MAIN



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AOZ2262_1D35V_VRAM
Size / Document Number	Custom / Strongbow_KL
Rev	1
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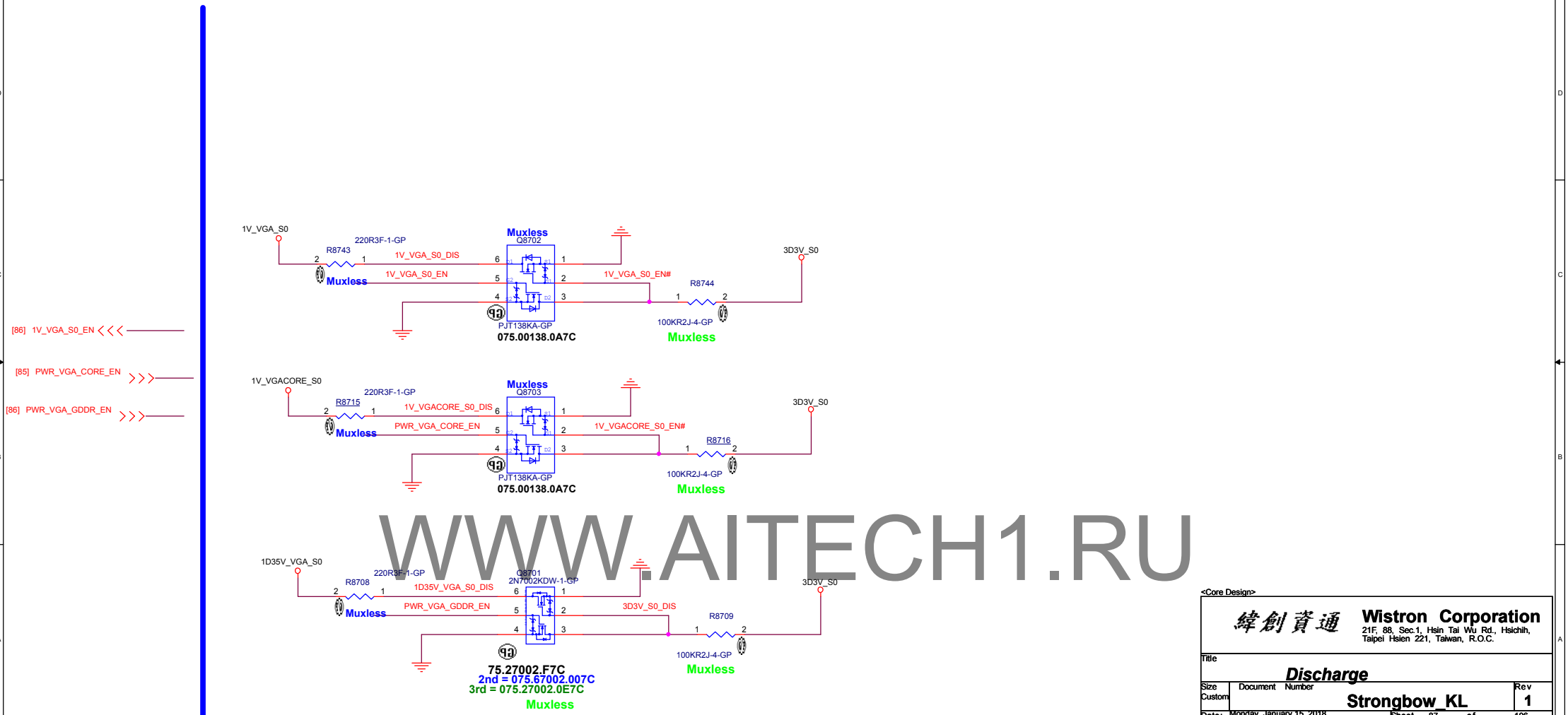

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Discharge

Size	Document Number	Rev
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<Core Design>

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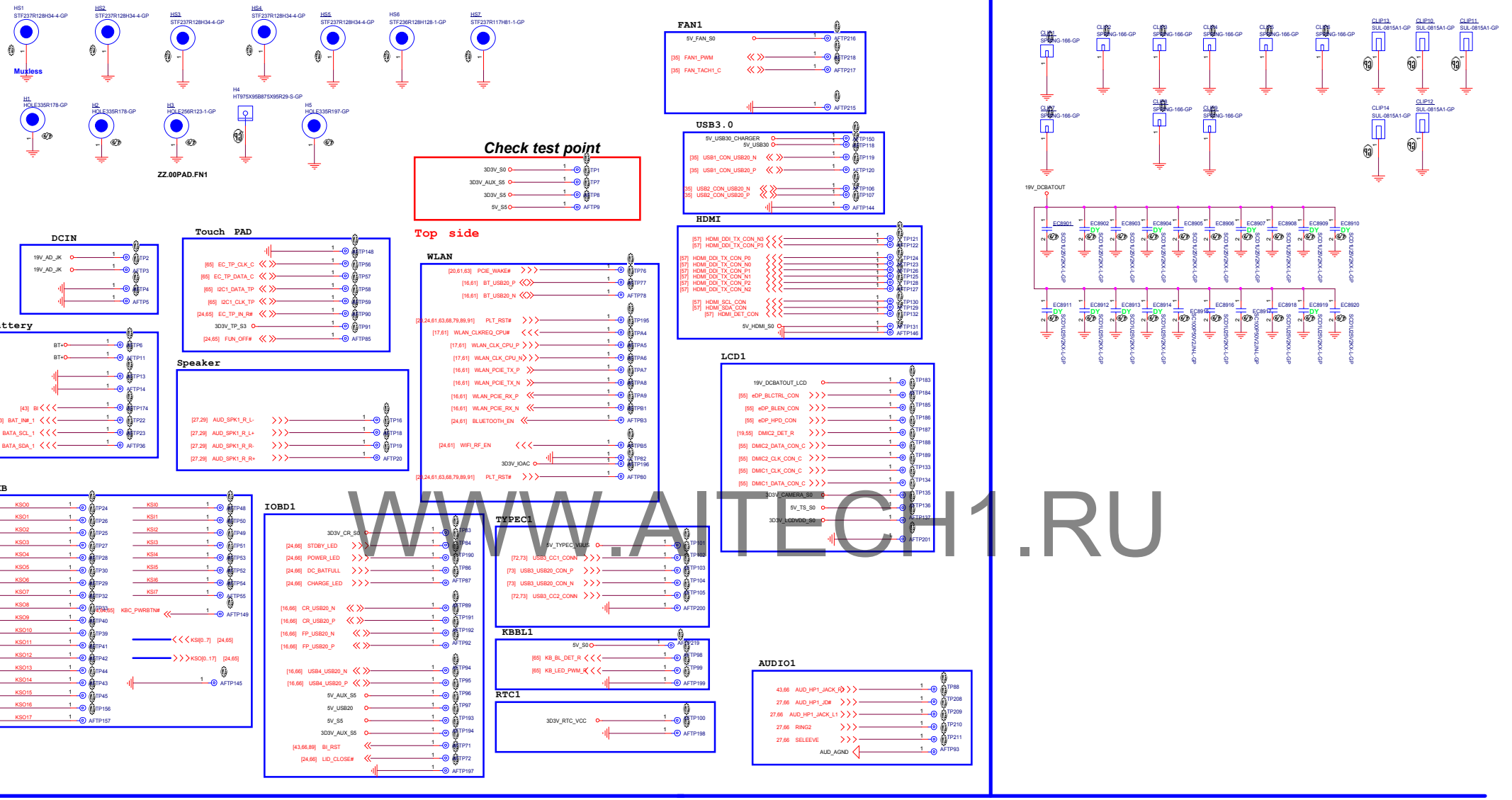
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	N16 Power	
Size: Custom	Document Number: Strongbow_KL	Rev: 1
Date: Thursday, January 11, 2018	Sheet 88 of 106	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***Reserved***

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A4	Strongbow_KL	1

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[19,24,68] LPC_AD_CPU_P0
[19,24,68] LPC_AD_CPU_P1
[19,24,68] LPC_AD_CPU_P2
[19,24,68] LPC_AD_CPU_P3

[19] LPC_CLK_TPM
[19,24,68] LPC_FRAME#_CPU
[20,24,61,63,68,79,89] PLT_RST#
[19,24,68] INT_SERIRQ
[19,24] PM_CLKRUN#_EC

[20,24,40,60] PM_SLP_S0#

3D3V_S5 3D3V_S0

C9101 SCD1U16V2KX-L-GP
C9102 SC10U6D3V3KX-L-GP
C9103 SCD1U16V2KX-L-GP
C9104 SCD1U16V2KX-L-GP

TPM TPM TPM TPM

3D3V_S0

R9103 4K7R2J-L-GP DY
TPM_PP
R9104 4K7R2J-L-GP
TPM

3D3V_S0

R9107 0R0402-PAD

3D3V_S5

R9105 0R0402-PAD

U9101

3D3V_TPM_VDD
VSBD

VDD 8
VDD 14
VHIO 22
VHIO
VSB 1

LPC_AD_CPU_P0 24 LAD0/MISO
LPC_AD_CPU_P1 21 LAD1/MOSI
LPC_AD_CPU_P2 18 LAD2/SPI_IRQ#
LPC_AD_CPU_P3 15 LAD3

PLT_RST# 17 LRESET#/SPI_RST#/SRESET#
LPC_CLK_TPM 19 LCLK/SCLK
LPC_FRAME#_CPU 20 LFRAME#/SCS#
INT_SERIRQ 27 SERIRQ
TP9101 1 LPCPD# 28 LPCPD#

TPM_PP 4 PP
5 TEST

SDA/GPIO0 29
GPIO1/SCL 30
GPX/GPIO2 3
GPIO3/BADD 6
CLKRUN#/GPIO4/SINT# 13
RESERVED#12 12

NC#2 2
NC#7 7
NC#10 10
NC#11 11
NC#25 25
NC#26 26
NC#31 31

GND 9
GND 16
GND 23
GND 32
GND 33
GND

GPX/GPIO2 2 R9106 1 PM_SLP_S0#
0R0402-PAD-1-GP

PM_CLKRUN#_EC

NPCT650ABBYX-GP

TPM

071.00650.0N03

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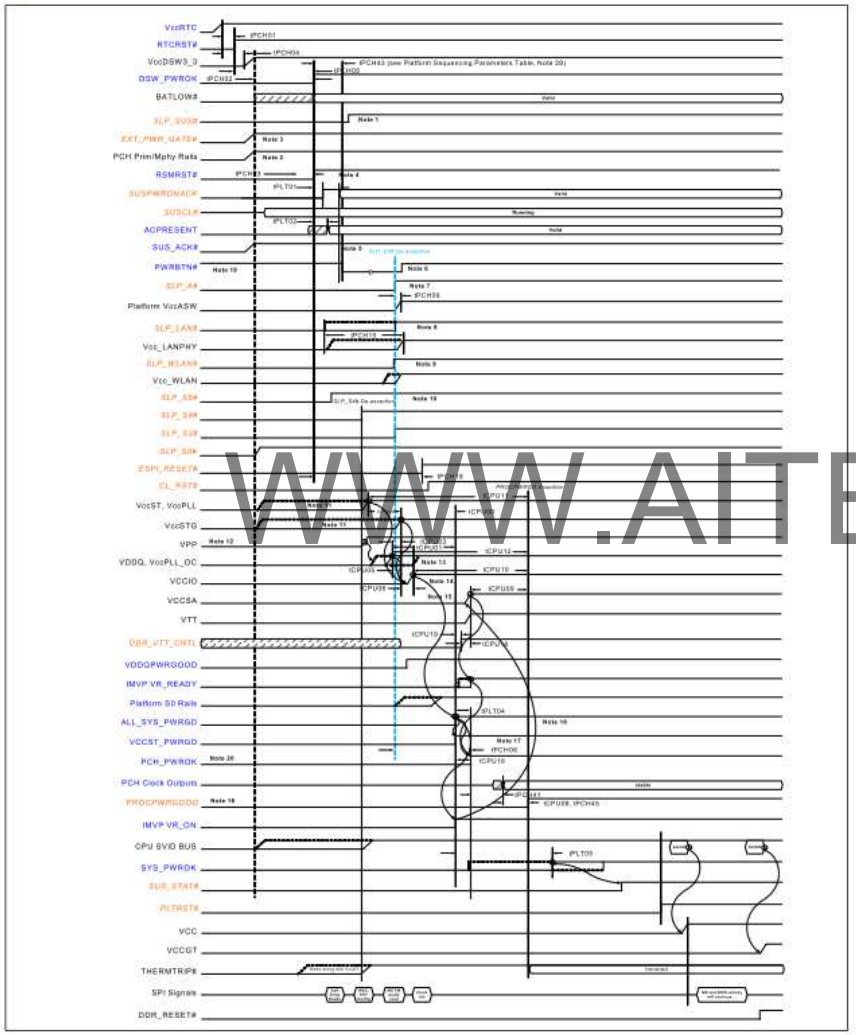
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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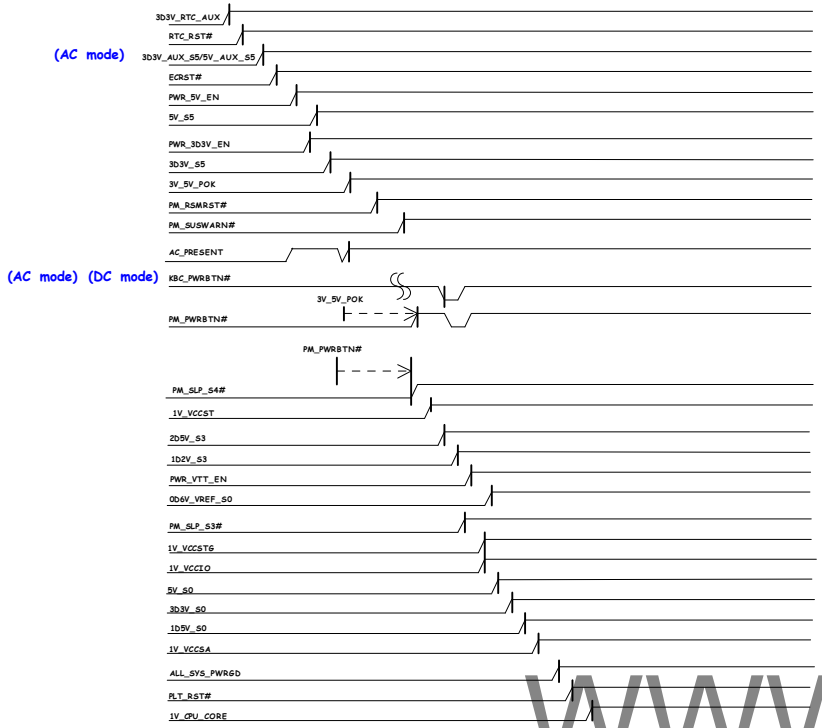
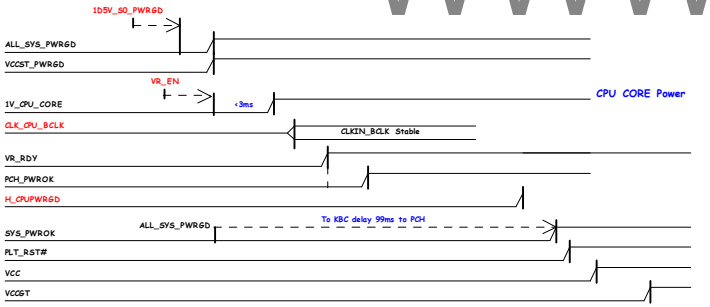
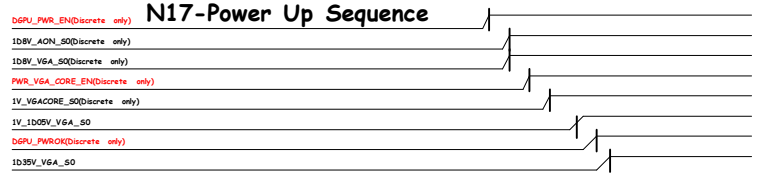
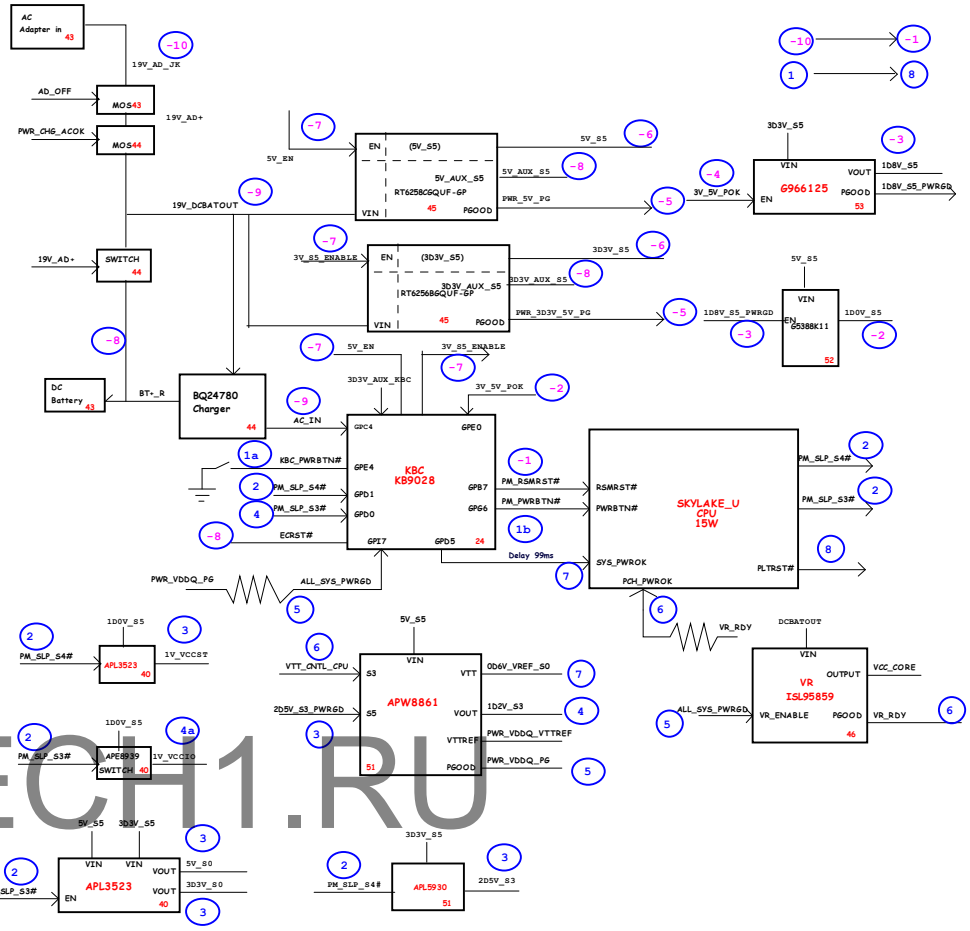
Intel-Power Up Sequence

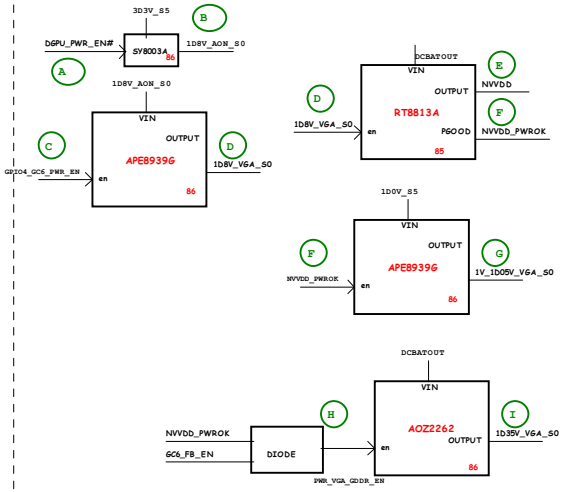




N17-Power Up Sequence







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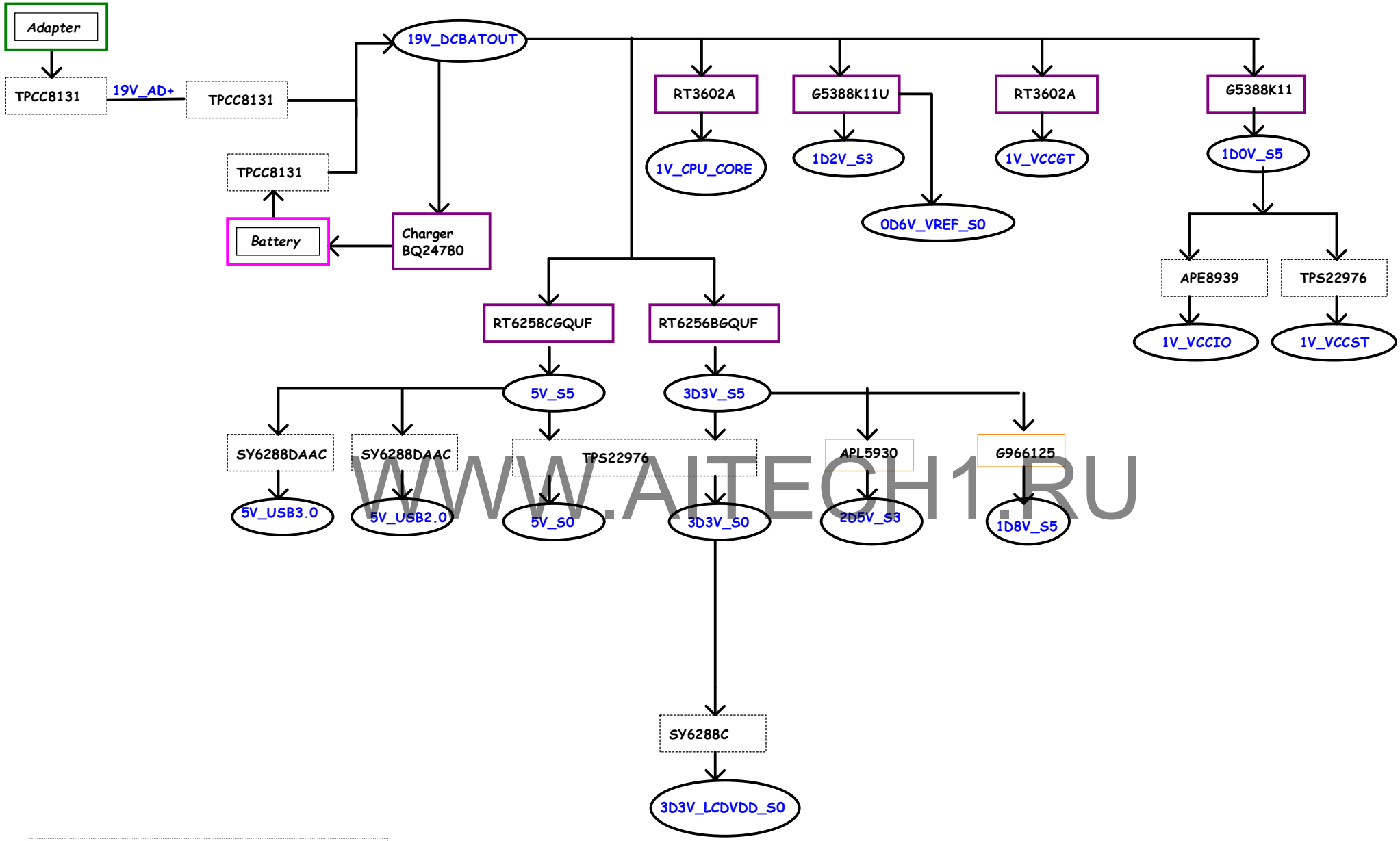

Power Shape

Regulator	LDO	Switch

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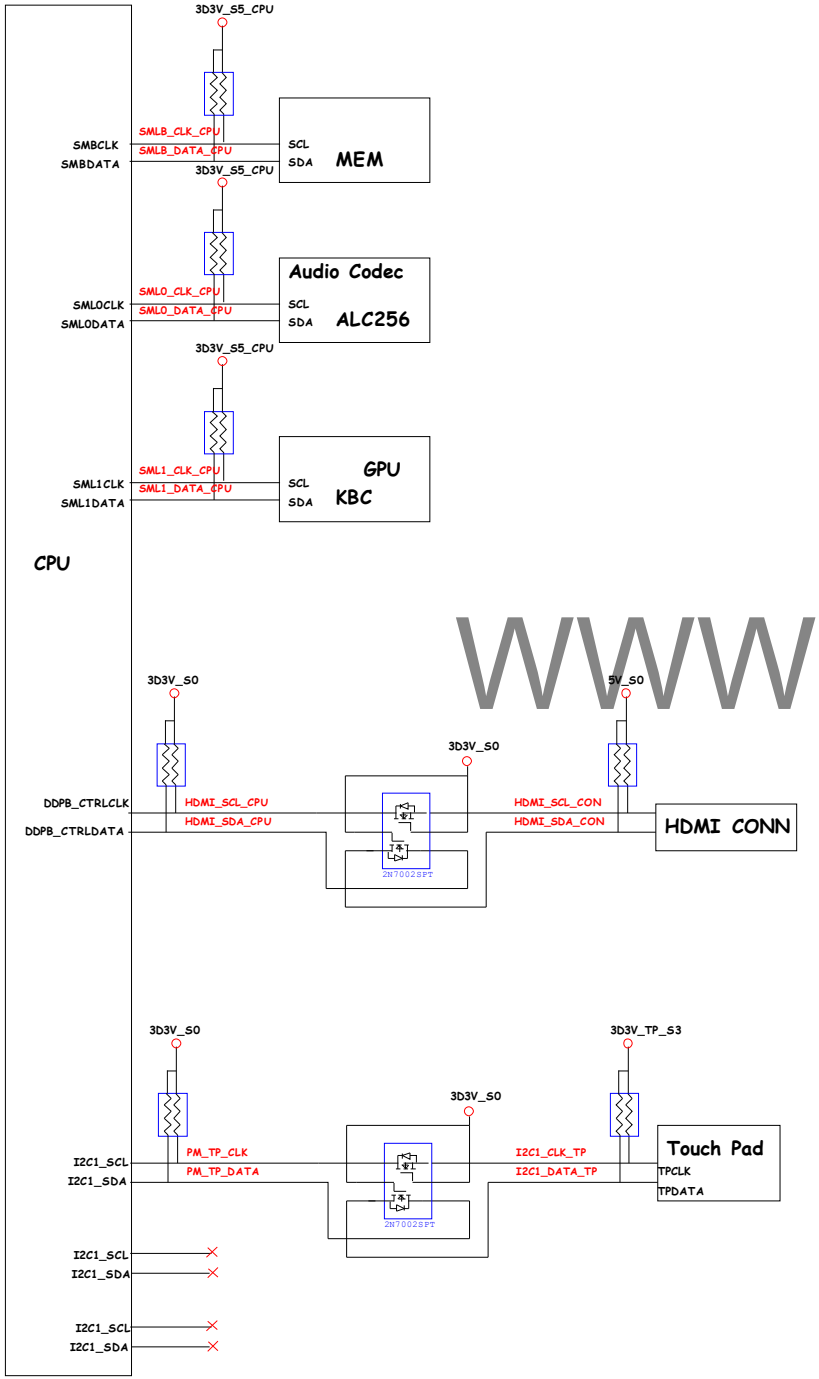
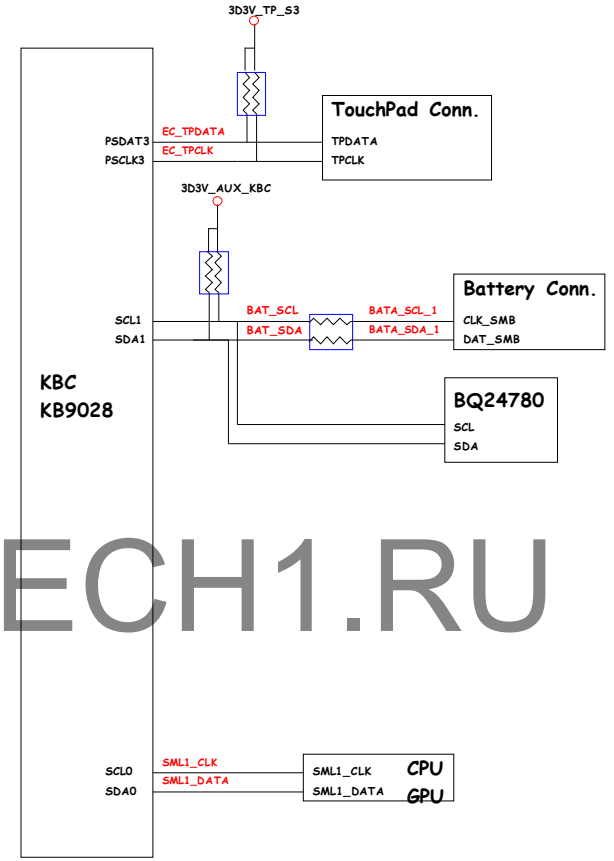
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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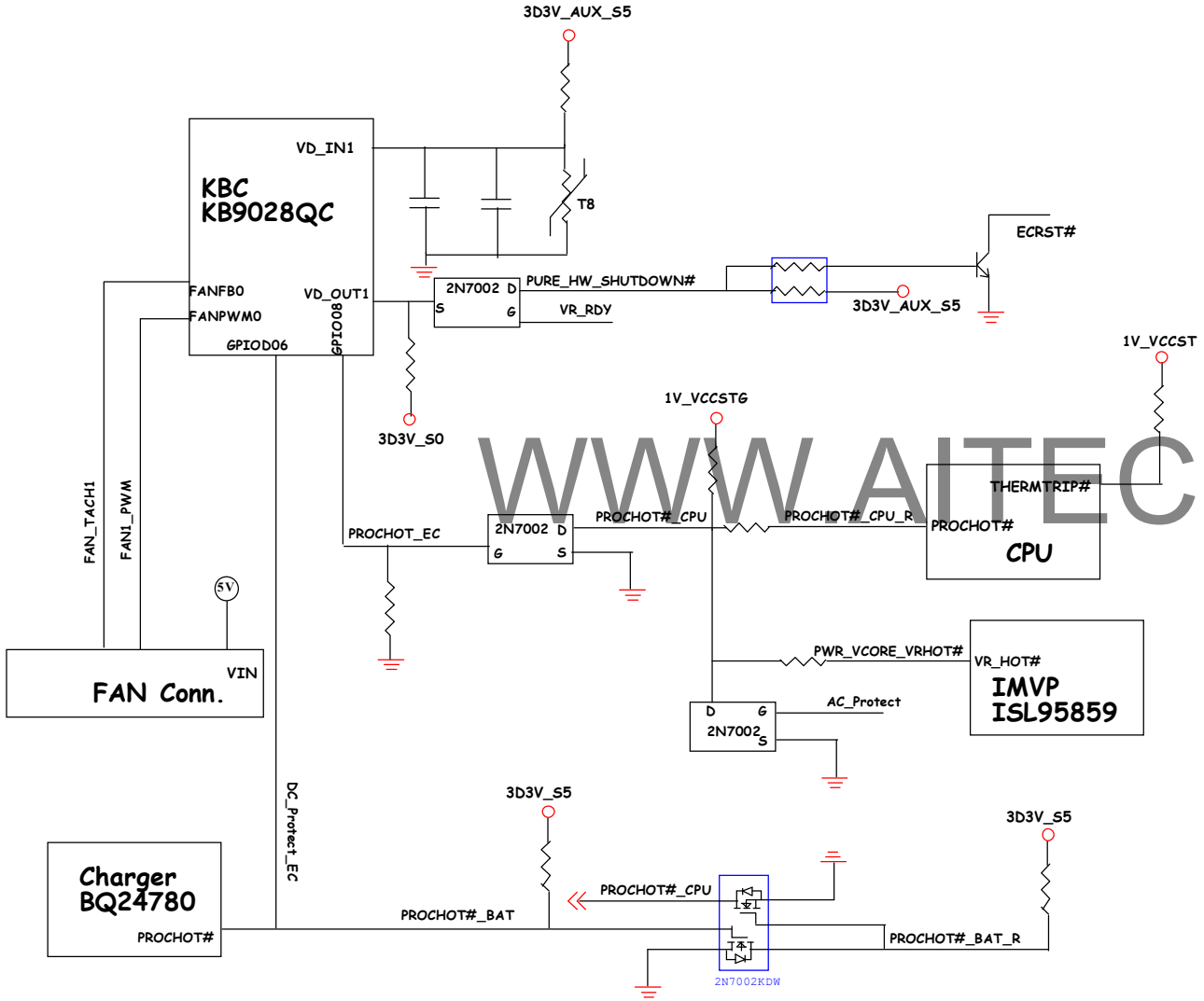
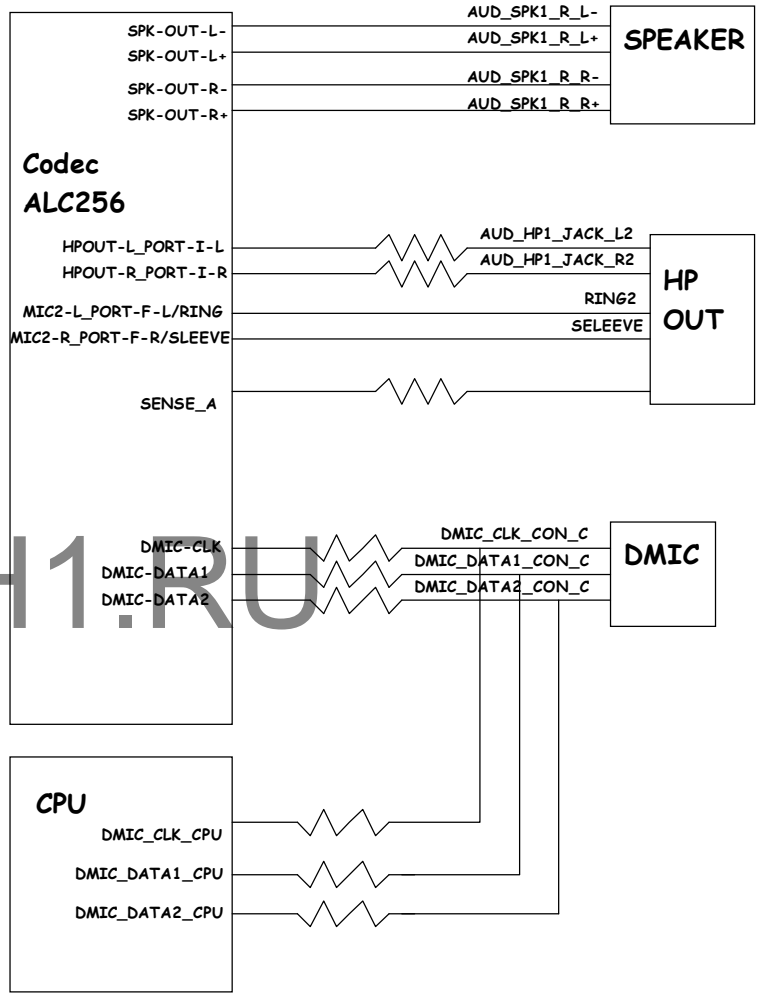
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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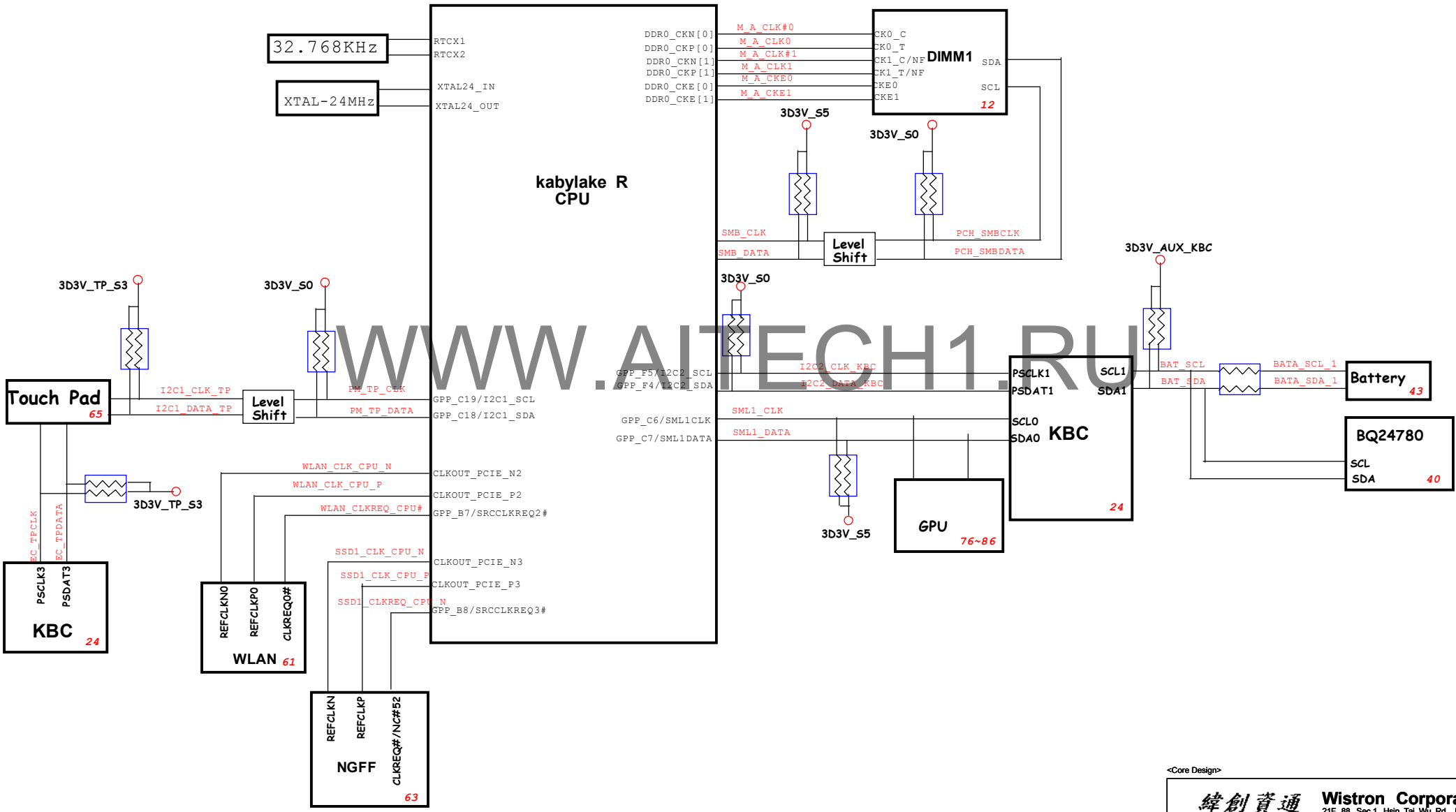
CLOCK BLOCK DIAGRAM



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Title: CLK Block

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